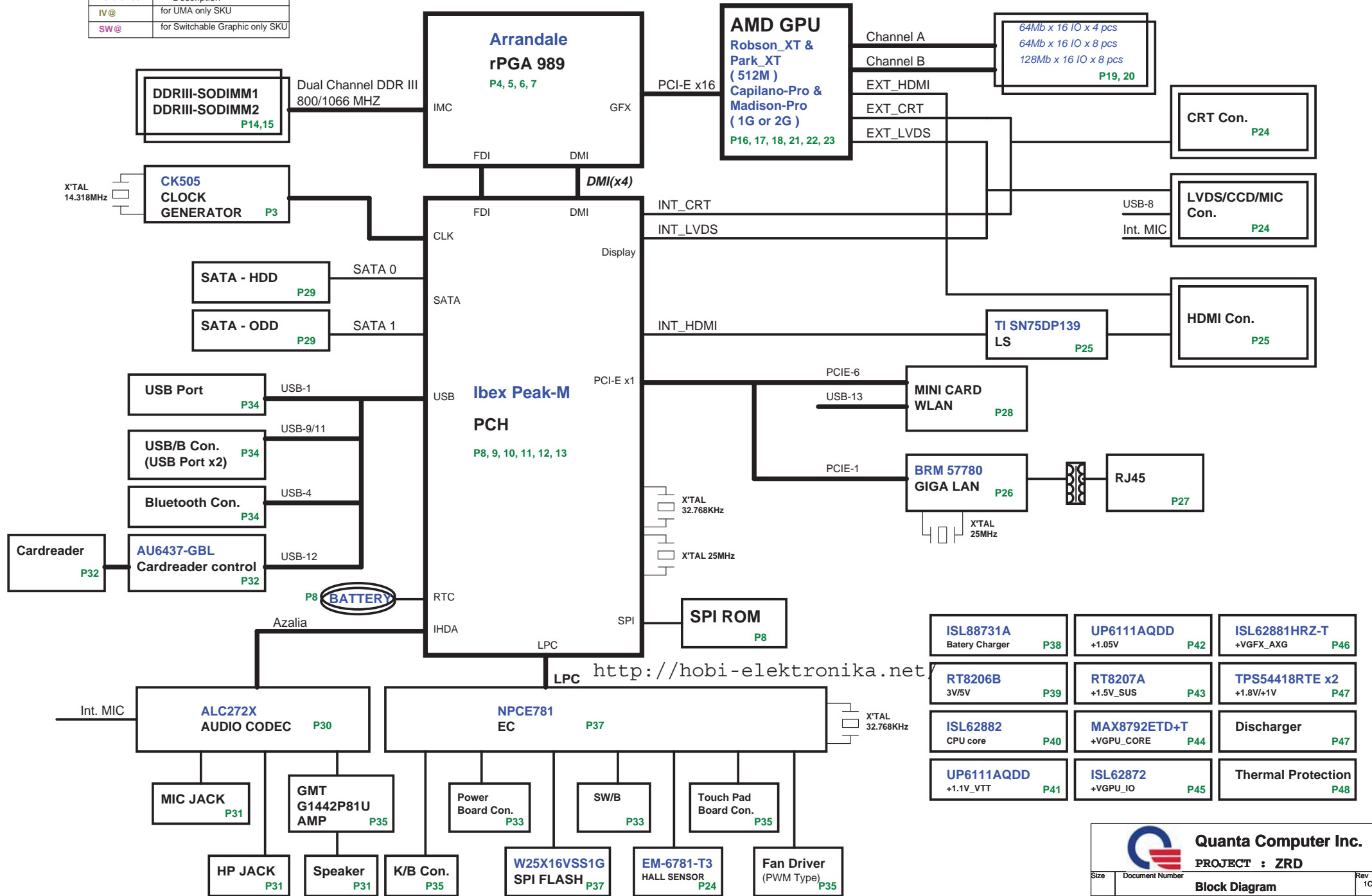


# HM55\_CP (ZRD) SYSTEM BLOCK DIAGRAM

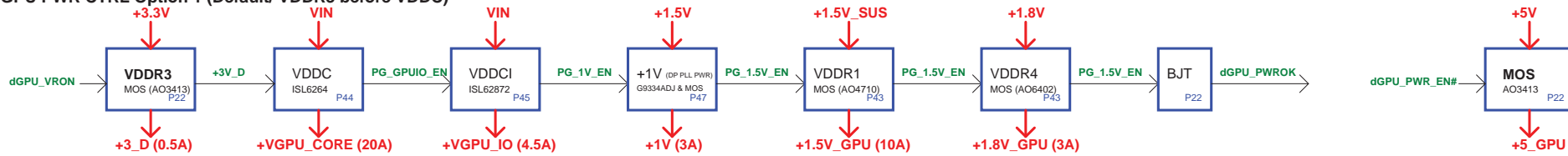
BOM Option Table

| Reference | Description                     |
|-----------|---------------------------------|
| IV@       | for UMA only SKU                |
| SW@       | for Switchable Graphic only SKU |

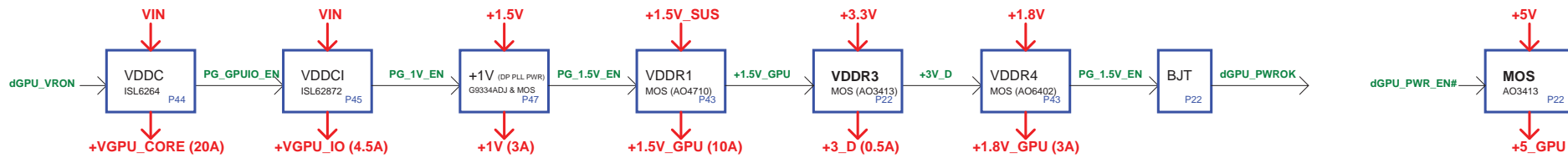


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### GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



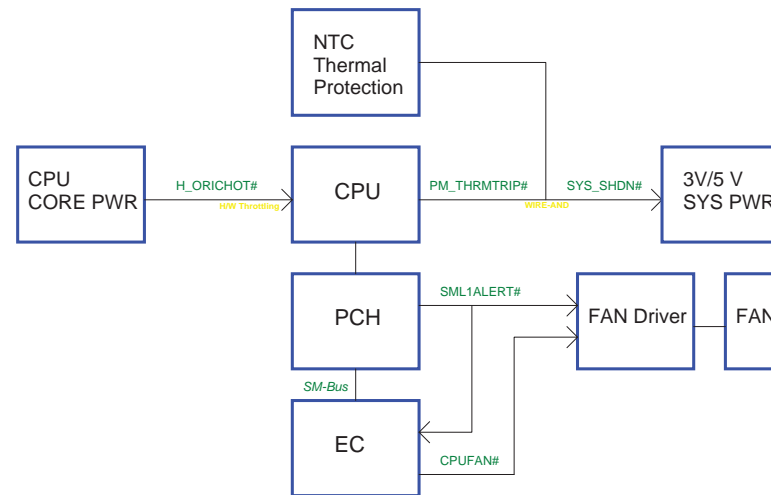
### GPU PWR CTRL Option 2 (VDDR3 after VDDC)



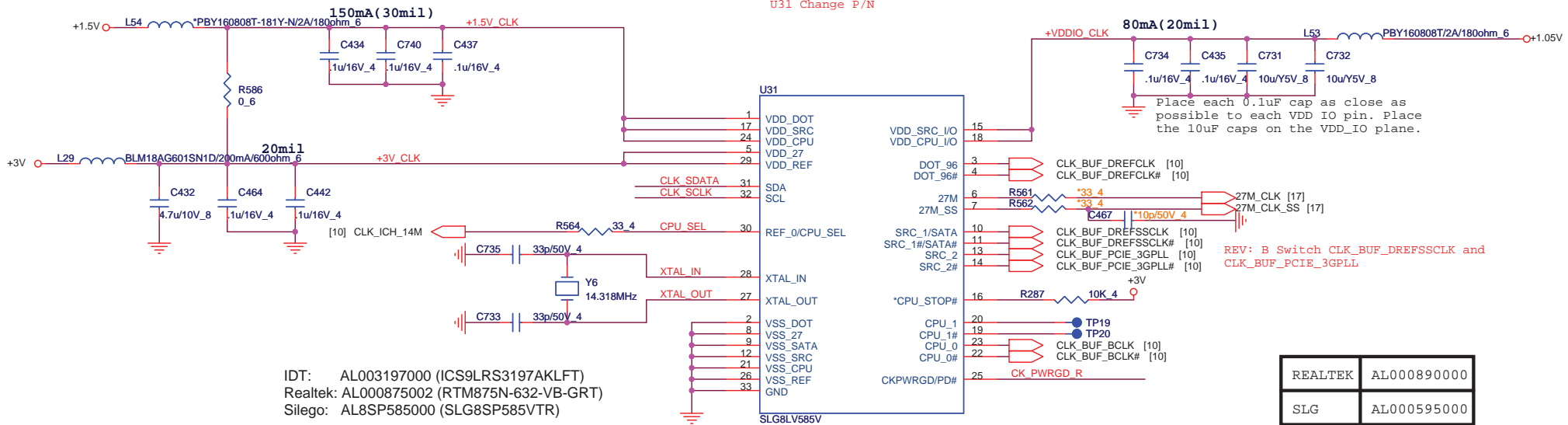
### Power States

| POWER PLANE    | VOLTAGE         | DESCRIPTION                        | CONTROL SIGNAL | ACTIVE IN       |
|----------------|-----------------|------------------------------------|----------------|-----------------|
| VIN            | +10V~+19V       | MAIN POWER                         | ALWAYS         | ALWAYS          |
| +VCCRTC        | +3V~+3.3V       | RTC POWER                          | ALWAYS         | ALWAYS          |
| +3VPCU         | +3.3V           | EC POWER                           | ALWAYS         | ALWAYS          |
| +5VPCU         | +5V             | CHARGE POWER                       | ALWAYS         | ALWAYS          |
| +15V           | +15V            | CHARGE PUMP POWER                  | ALWAYS         | ALWAYS          |
| +3V_S5         | +3.3V           | LAN/BT/CIR POWER                   | S5_ON          | S0-S5           |
| +5V_S5         | +5V             | USB POWER                          | S5_ON          | S0-S5           |
| +5V            | +5V             | HDD/ODD/Codec/TP/CRT/HDMI POWER    | MAINON         | S0              |
| +3V            | +3.3V           | PCH/GPU/Peripheral component POWER | MAINON         | S0              |
| +1.5VSUS       | +1.5V           | CPU/SODIMM CORE POWER              | SUSON          | S0-S3           |
| +0.75V_DDR_VTT | +0.75V          | SODIMM Termination POWER           | MAINON         | S0              |
| +VGFX_AXG      | variation       | Internal GPU POWER                 | GFX_ON         | S0              |
| +1.8V          | +1.8V           | CPU/PCH/Braidwood POWER            | MAINON         | S0              |
| +1.5V          | +1.5V           | MINI CARD/NEW CARD POWER           | MAINON         | S0              |
| +1.1V_VTT      | +1.05V or +1.1V | CPU VTT POWER                      | MAINON         | S0              |
| +1.05V         | +1.05V          | PCH CORE POWER                     | MAINON         | S0              |
| +VCC_CORE      | variation       | CPU CORE POWER                     | VRON           | S0              |
| LCDVCC         | +3.3V           | LCD POWER                          | LVDS_VDDEN     | S0              |
| +5V_GPU        | +5V             | SWITCHABLE PWM IC POWER            | dGPU_PWR_EN#   | Discrete enable |
| +GPU_CORE      | +0.9V~+1.1V     | GPU CORE POWER                     | +3V_D          | Discrete enable |
| +GPU_IO        | +0.9V~+1.1V     | GPU I/O POWER                      | PG_GPUIO_EN    | Discrete enable |
| +1.5V_GPU      | +1.5V           | VRAM CORE POWER                    | PG_1.5V_EN     | Discrete enable |
| +1.8V_GPU      | +1.8V           | GPU_CRE/LVDS/PLL POWER             | +1.5V_GPU      | Discrete enable |
| +1V            | +1V             | DP/PEG POWER                       | PG_1V_EN       | Discrete enable |

### Thermal Follow Chart

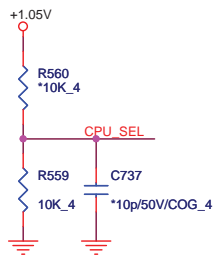


6/21 add R586 for 3V CLK gen  
Un-stuff L54  
U31 Change P/N



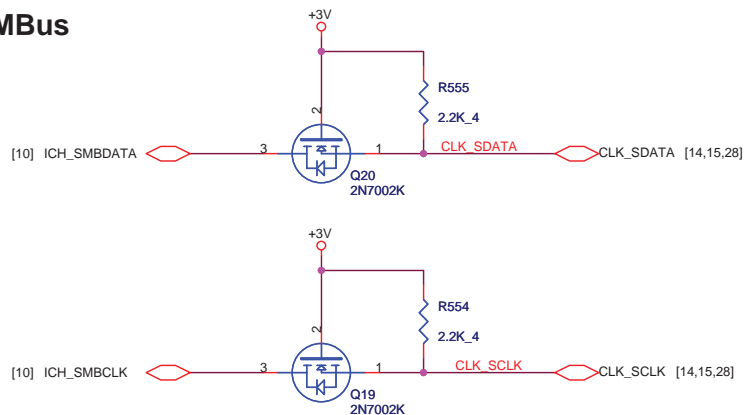
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### CPU\_CLK select

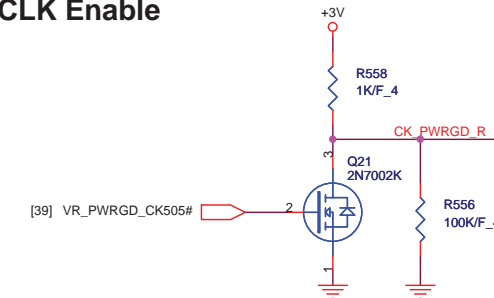


|         | 0                       | 1             |
|---------|-------------------------|---------------|
| CPU_SEL | CPU0/1=133MHz (default) | CPU0/1=100MHz |

### SMBus

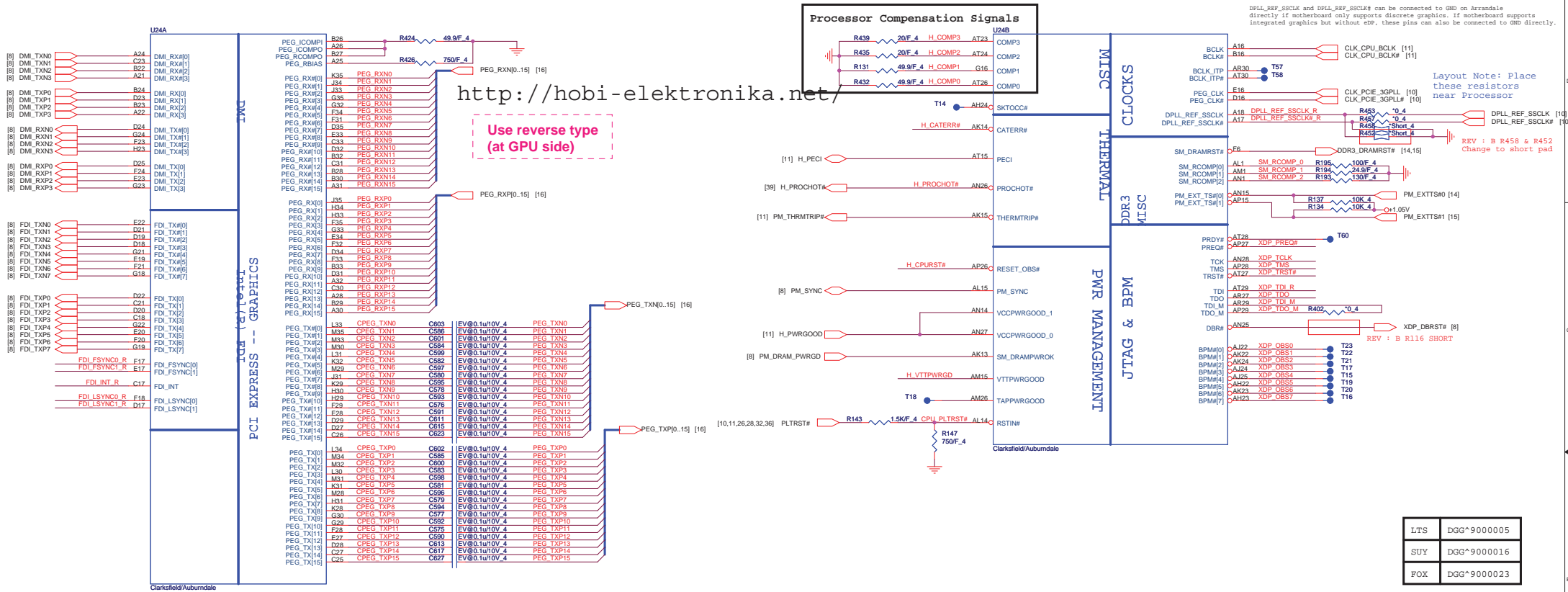


### CLK Enable



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|       |                          |               |
|-------|--------------------------|---------------|
| Size  | Document Number          | Rev           |
|       | <b>Clock Generator</b>   | 1C            |
| Date: | Wednesday, July 21, 2010 | Sheet 3 of 46 |

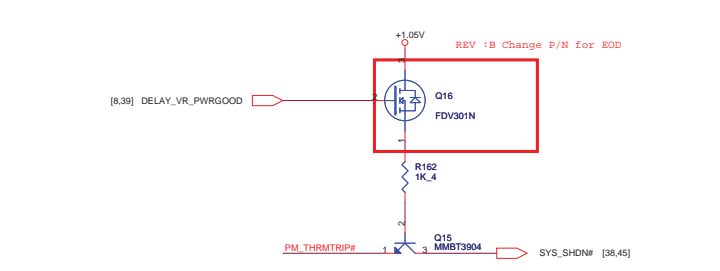


<http://hobi-elektronika.net/>

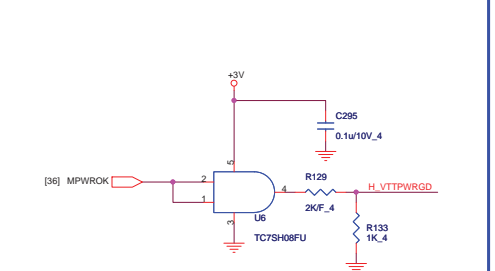
Use reverse type (at GPU side)

|     |             |
|-----|-------------|
| ITS | DG9*9000005 |
| SUY | DG9*9000016 |
| POX | DG9*9000023 |

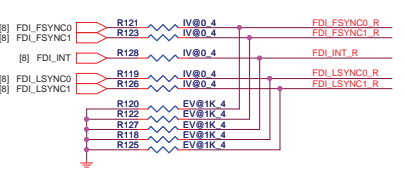
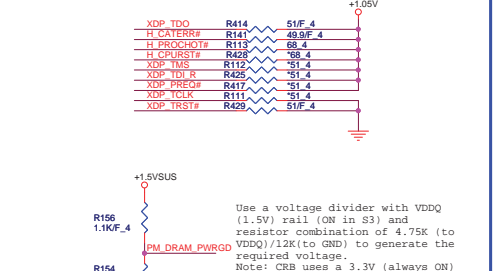
**Thermaltrip protect**



**VTT PWR\_Good**



**Processor pull-up**

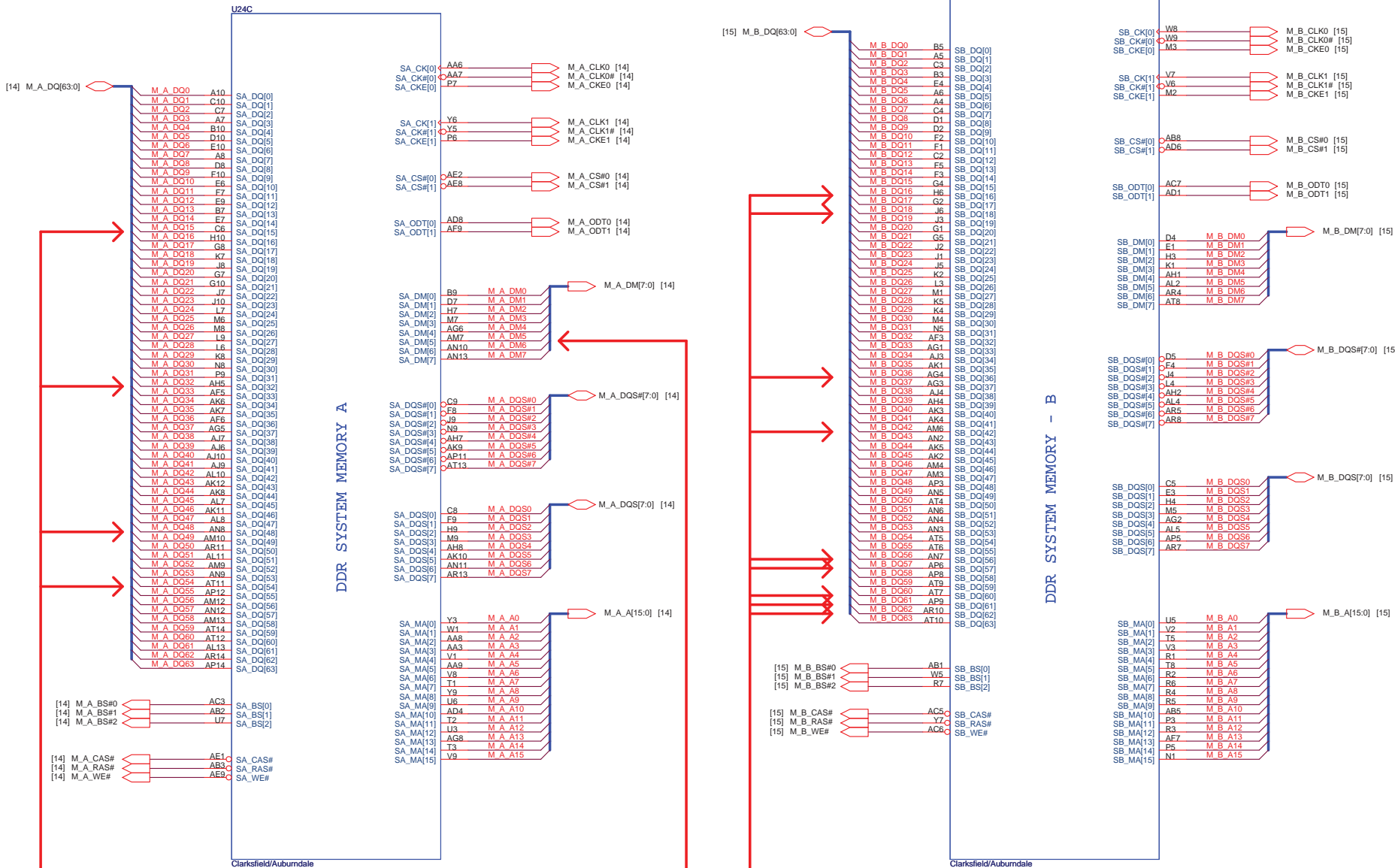


<The GFX\_IMON, FDI\_FSYNCO[0], FDI\_FSYNCO[1], FDI\_LSYNCO[0], FDI\_LSYNCO[1], and FDI\_INT>Note that if these signals are left as no connect, there are no functional impacts, but a small amount of power (~15 mW) maybe wasted.

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|       |                          |               |
|-------|--------------------------|---------------|
| Size  | Document Number          | Rw            |
|       | AUBURND 1/4              | 1C            |
| Date: | Wednesday, July 21, 2010 | Sheet 4 of 46 |

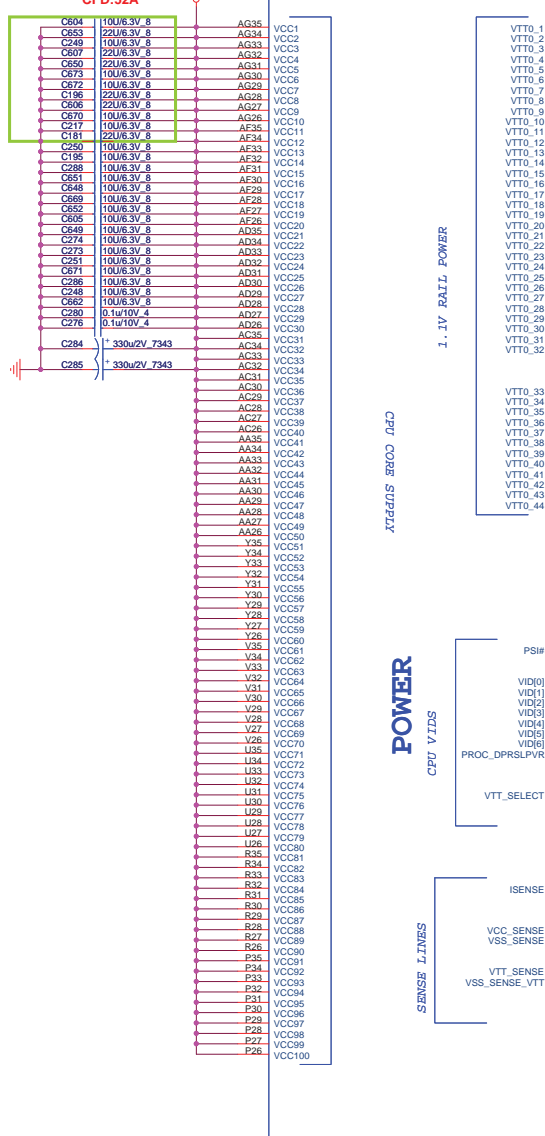
# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Channel A DQ[15,32,48,54], DM[5]  
Requires minimum 12mils spacing  
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]  
Requires minimum 12mils spacing  
with all other signals, including data signals.

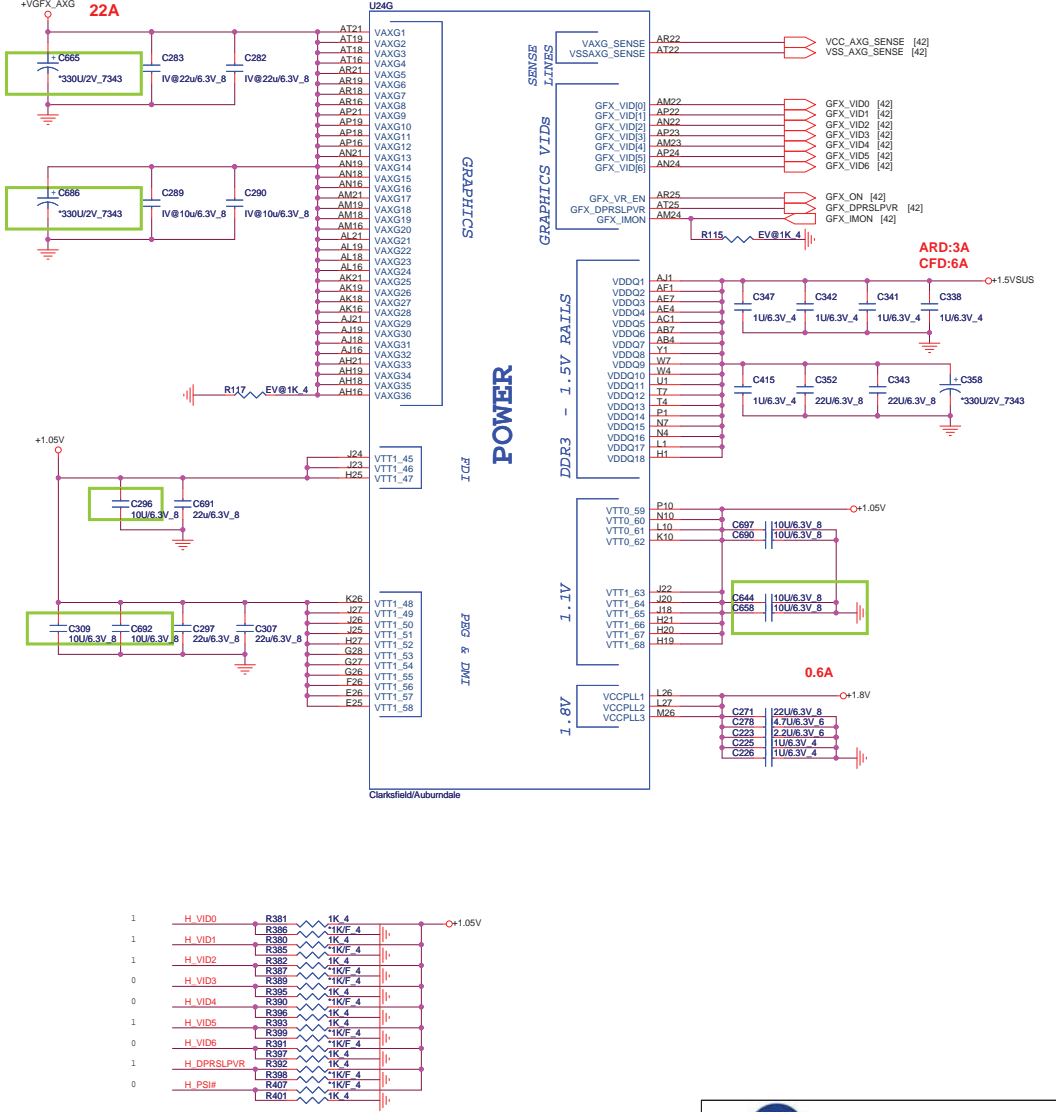
ARD:48A  
CFD:52A



VTT Rail Values are  
Auburndale VTT=1.05V  
Clarksfield VTT=1.1V

AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)

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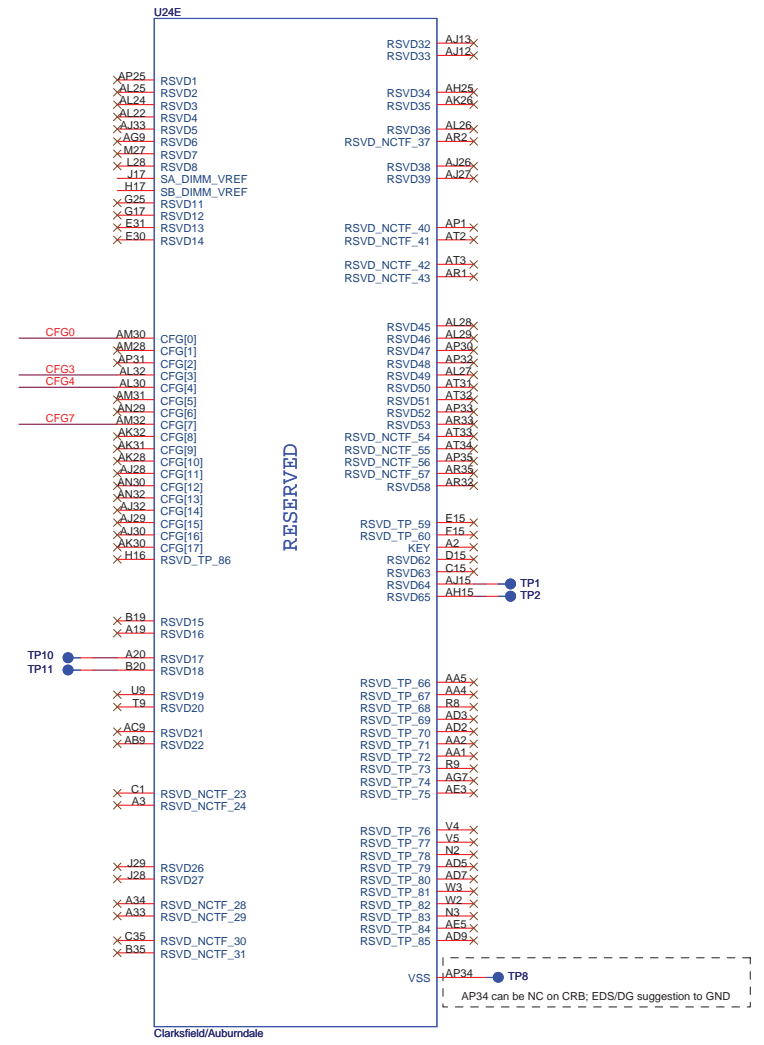
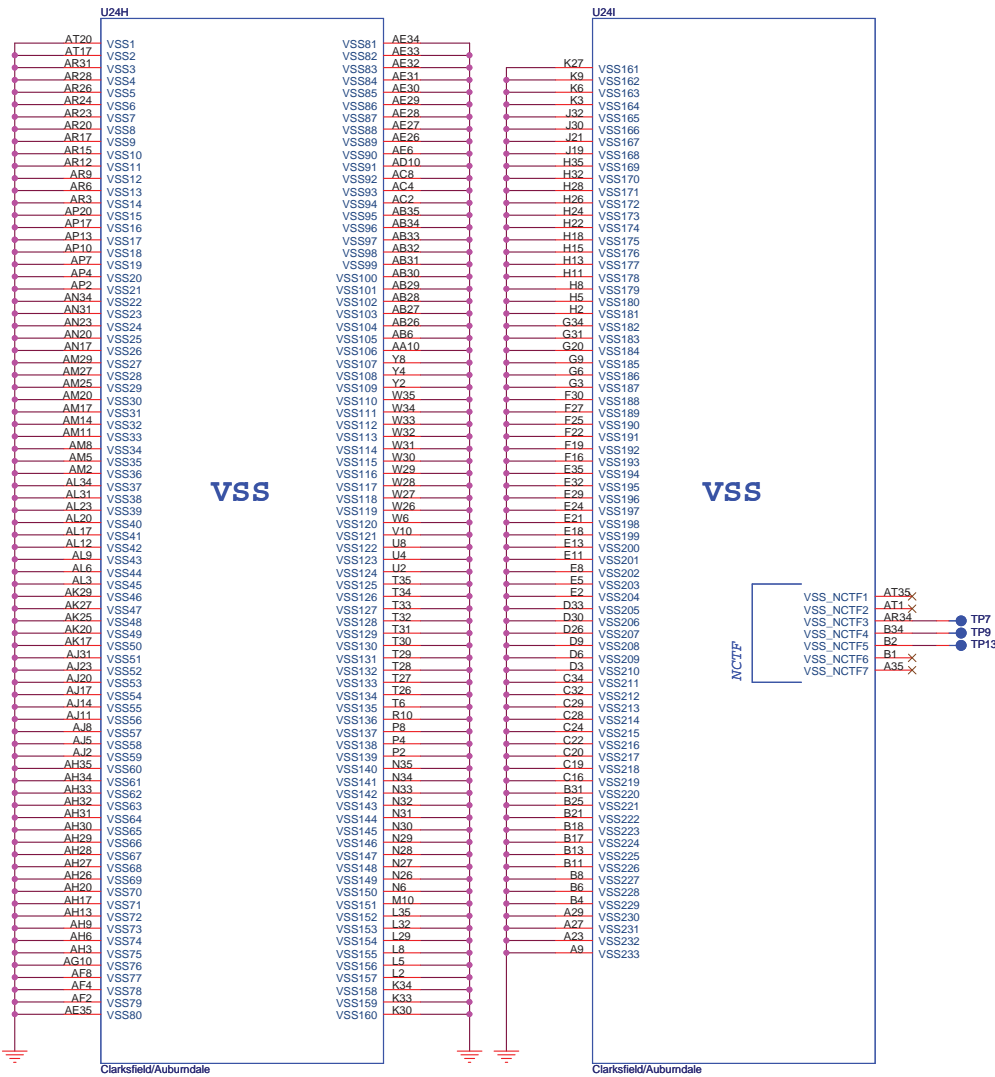
AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

HFC: For Validating IMVP VR R6451 should be STUFF and R2N1 NO\_STUFF  
HFM\_VID : Max 1.4V  
LFM\_VID : Min 0.65V

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AUBURND 3/4 (PWR)  
Date: Wednesday, July 21, 2010 Sheet: 6 of 46

# AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

# AUBURNDALE/CLARKSFIELD PROCESSOR ( RESERVED, CFG)



## Processor Strapping

|  | 1   | 0  | DEFAULT |  |
|--|---|--|---------|--|
| CFG0<br>(PCI-Epress<br>Configuration Select)   | Single PEG  | Bifurcation enabled  | 1       |  |
| CFG3<br>(PCI-Epress Static<br>Lane Reversal)   | Normal Operation  | Lane Numbers Reversed  | 1       |  |
| CFG4<br>(Embedded<br>Display Port Presence)  | Disabled; No Physical Display Port<br>attached to Embedded Display Port | Enabled; An external Display port<br>device is connected to the Embedded<br>Display port | 1       |  |
| The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed. |   |  |         |  |

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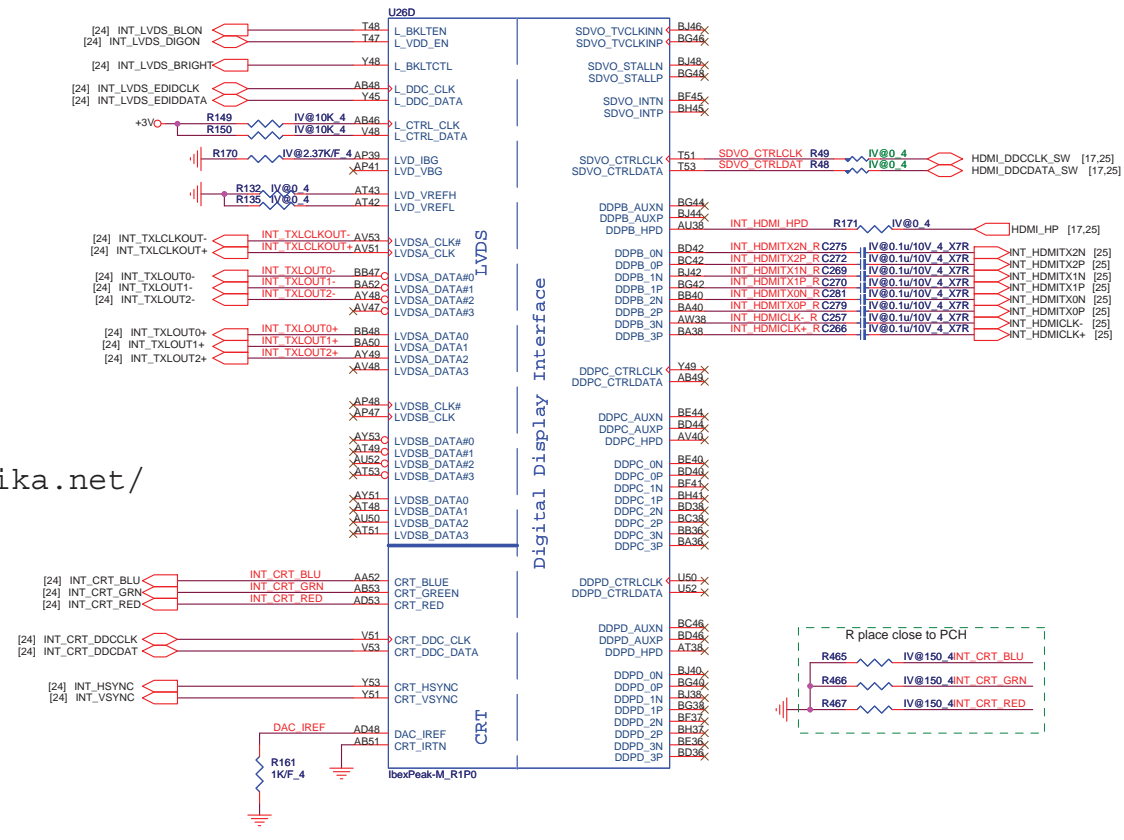
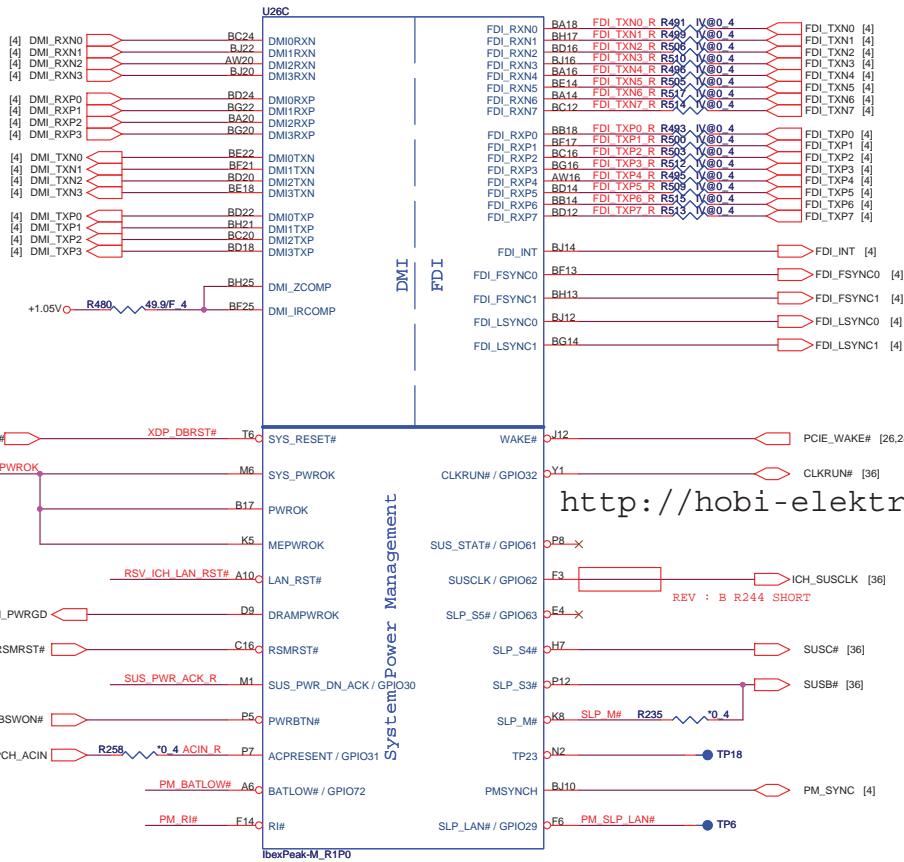
Size: \_\_\_\_\_ Document Number: **AUBURND4/4** Rev: 1C  
Date: Wednesday, July 21, 2010 Sheet 7 of 46

# IBEX PEAK-M (DMI, FDI, GPIO)

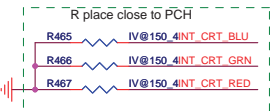
AC-coupling CAP place close to PCH

0-ohm resistor place close to PCH

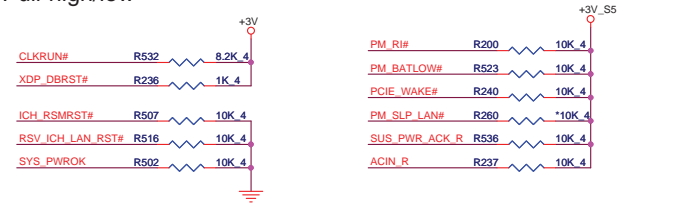
# IBEX PEAK-M (LVDS, DDI)



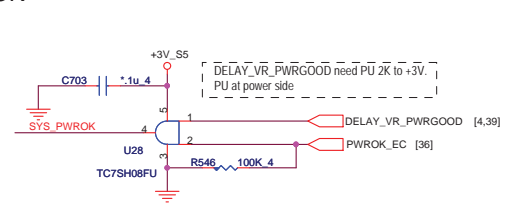
<http://hobi-elektronika.net/>



## PCH Pull-high/low



## System PWR\_OK

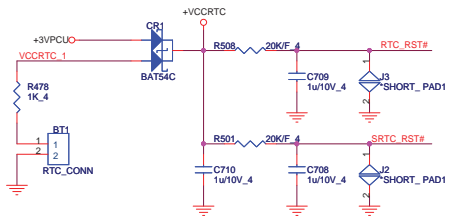


**Quanta Computer Inc.**  
PROJECT : ZRD

|       |                          |       |         |
|-------|--------------------------|-------|---------|
| Size  | Document Number          | Rev   |         |
|       | <b>IBEX PEAK-M 1/6</b>   | 1C    |         |
| Date: | Wednesday, July 21, 2010 | Sheet | 8 of 46 |

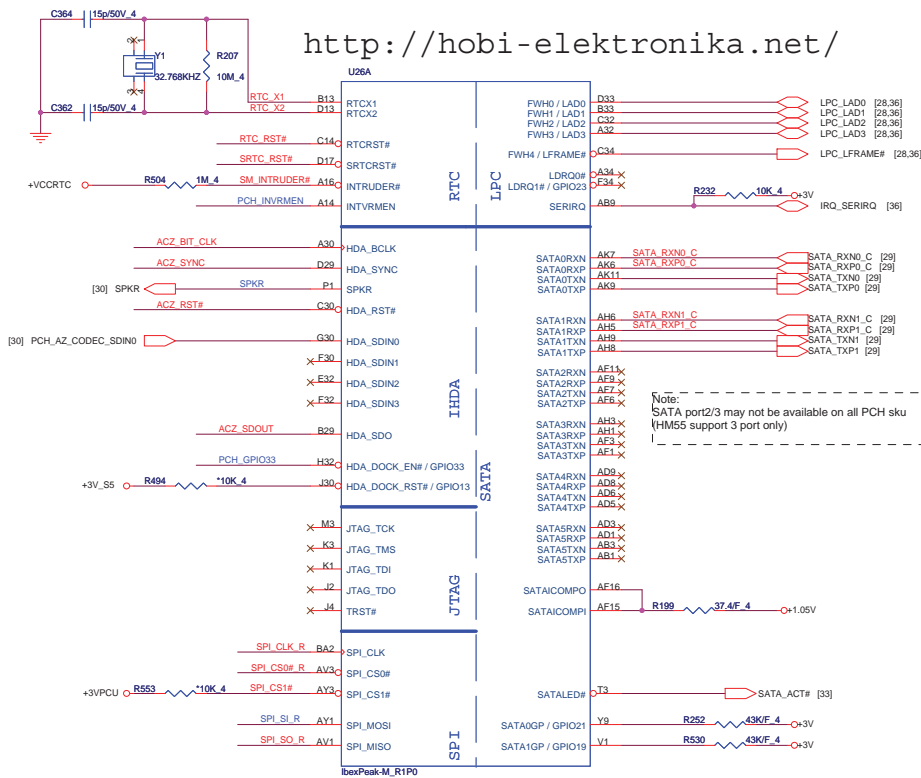


## RTC Circuitry

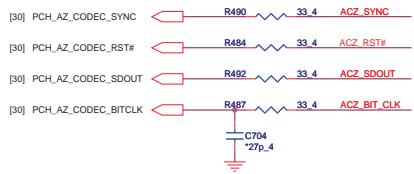


**HDA\_SYNC (PCH strap pin)**  
 Internal weak pull-down  
 VCCVRM=>1.8V (default)  
 external pull-up  
 VCCVRM=>1.5V

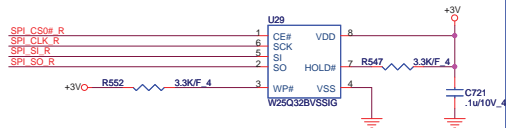
<http://hobi-elektronika.net/>



## HDA Bus

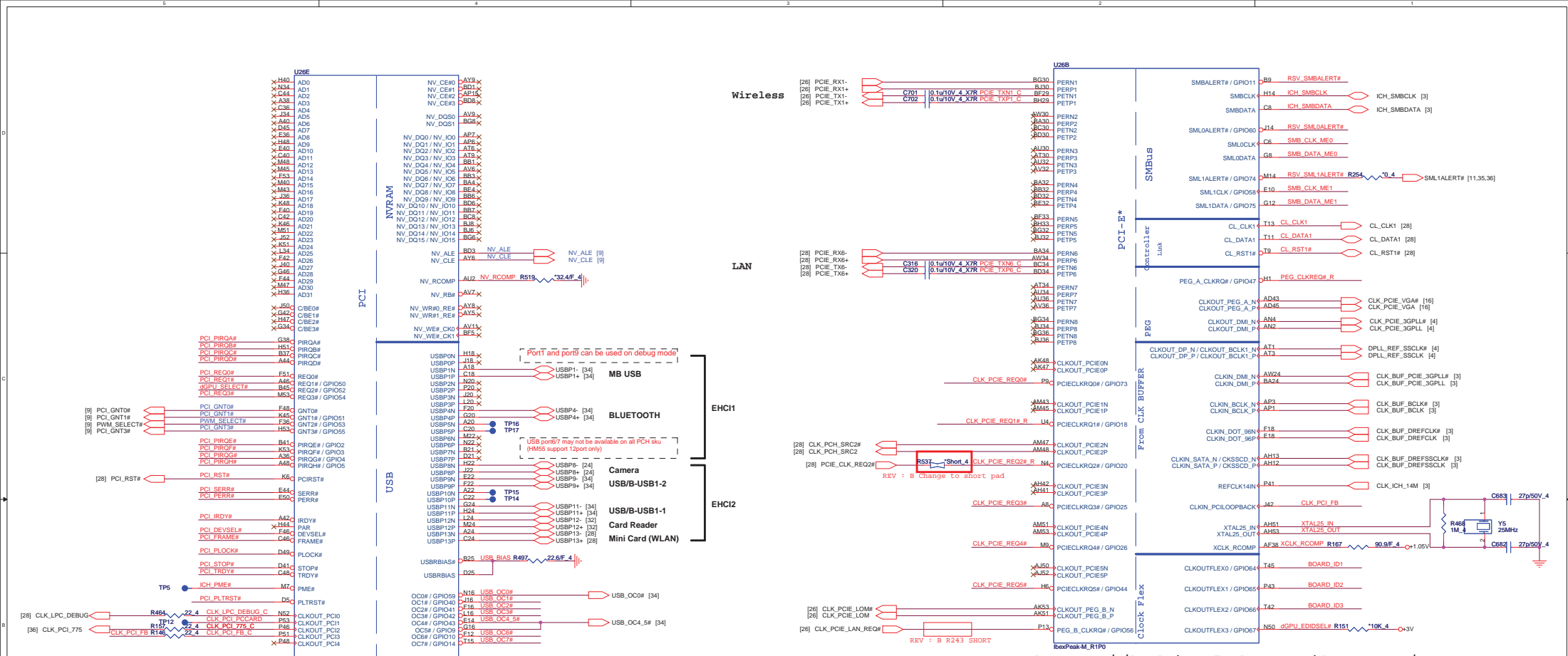


## PCH SPI

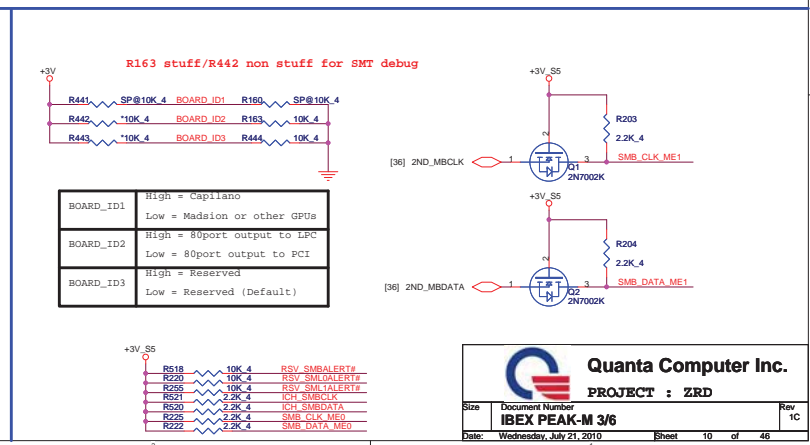
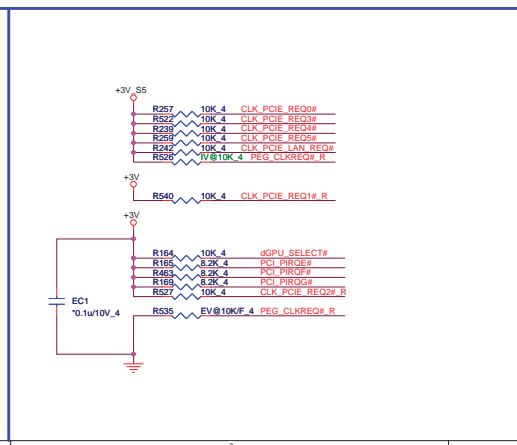
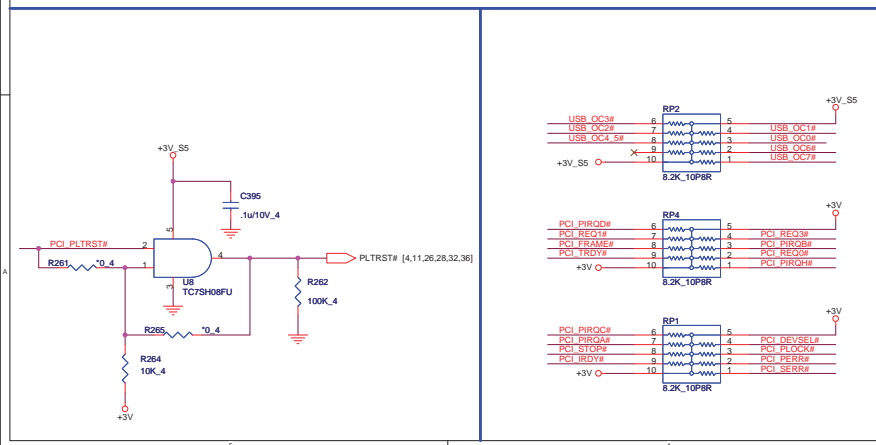


PCH Strap Pin Configuration Table-1

|                     |  |   |   |
|---------------------|--|---|---|
| INTVRMEN            | Integrated 1.05V VRM Enable / Disable                                | 1 = Integrated VRM is enabled<br>0 = Integrated VRM is disabled   | +VCCRTC ○ R511 330K 6 PCH_INVRMEN                           |
| SPI_MOSI            | TPM Functionality Disable  | 1 = Enabled<br>0 = Disabled   | +3V ○ R551 1K 4 SPI_SI_R                                    |
| SPKR                | Reboot option at power-up  | 0 = Default Mode (Internal weak Pull-down)<br>1 = No Reboot Mode with TCO Disabled  | +3V ○ R538 1K 4 SPKR  |
| HDA_DOCK_EN#/GPIO33 | Flash Descriptor Security Override                                   | 0 = Flash Descriptor Security will be overridden<br>1 = Security measure defined in the Flash Descriptor will be enabled.   | PCH_GPIO33 J1 1 2 'SHORT_PAD1                               |
| GNT0#, GNT1#        | Boot BIOS Strap  | (0,0) = LPC (0,1) = Reserved NAND<br>(1,0) = PCI (1,1) = SPI  | [10] PCH_GNT0# [10] PCH_GNT1# R158 1K 4 R157 1K 4 R159 1K 4 |
| GNT2#/GPIO53        | ESI Strap (Server Only)  | ESI compatible mode is for server platforms only  | [10] PWM_SELECT# R182 1K 4                                  |
| GNT3#/GPIO55        | Top-Block Swap Override  | 0 = Top Block Swap Mode<br>1 = Default Mode (Internal pull-up)  | [10] PCH_GNT3# R462 10K 4                                   |
| NV_ALE              | Intel® Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable | 1 = Enabled<br>0 = Disabled (Default)   | [10] NV_ALE R213 1K 4 +1.8V                                 |
| NV_CLE              | DMI Termination Voltage  | DMI termination voltage. Weak internal pull-up. Do not pull low.  | [10] NV_CLE R216 1K 4 +1.8V                                 |
| GPIO8               | Reserved   | This signal has a weak internal pull up. NOTE: This signal should not be pulled low   | [11] RSV_GPIO8 R215 10K 4 +3V_S5 R214 1K 4                  |
| GPIO15              | Reserved   | 0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality<br>1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality | [11] CR_WAKE# R256 1K 4 +3V_S5                              |
| GPIO27              | On-Die PLL Voltage Regulator <internal weak pull-up>                 | 0 = Disables the VccVRM.<br>1 = Enables the internal VccVRM to have a clean supply for analog rails.  | [11] PCH_GPIO27 R231 10K 4                                  |



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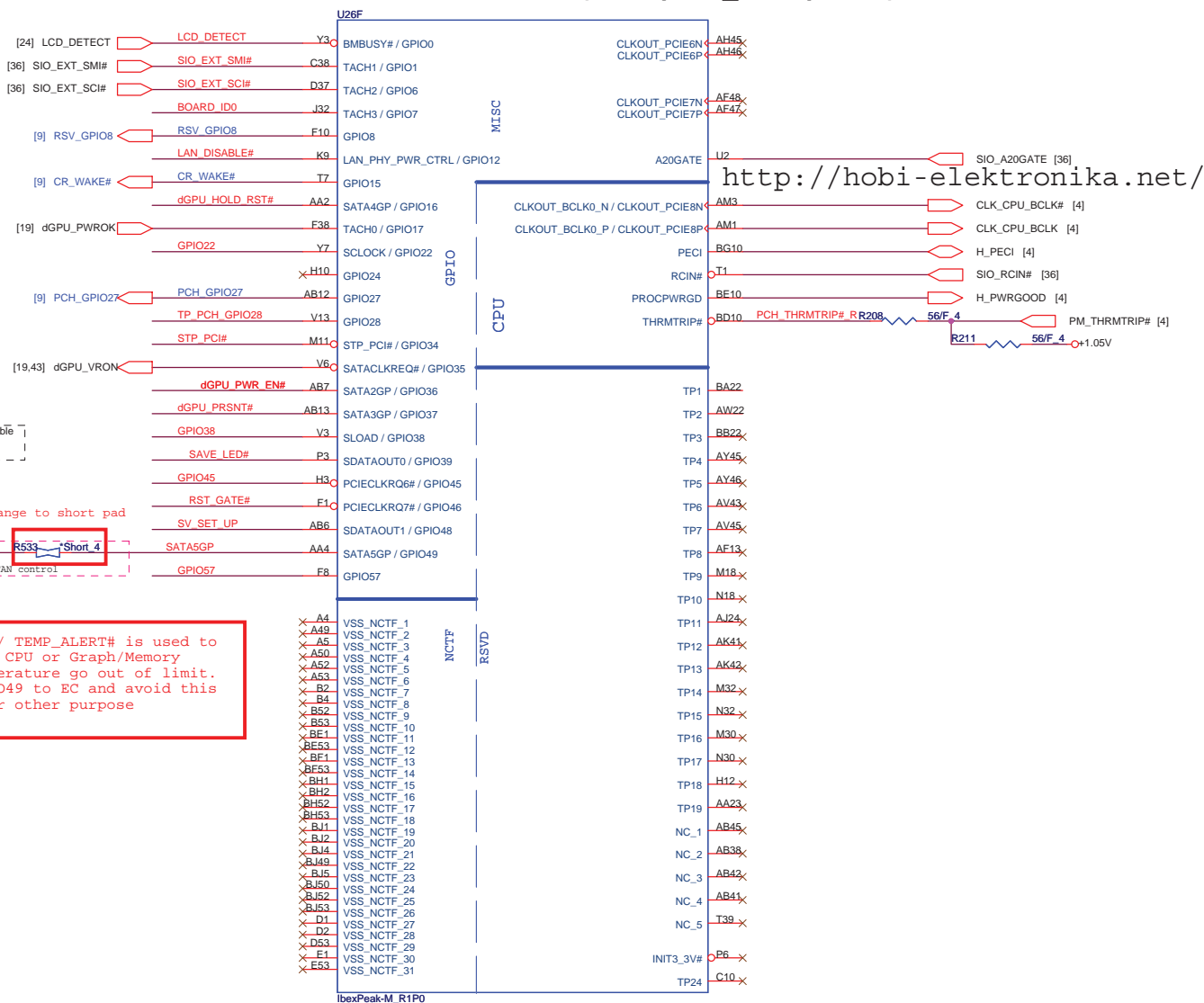
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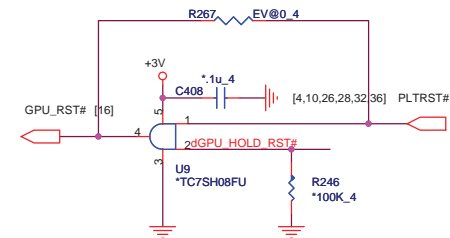
Size: Document Number: **IBEX PEAK-M 3/6** Rev: 1C

Date: Wednesday, July 21, 2010 Sheet: 10 of 46

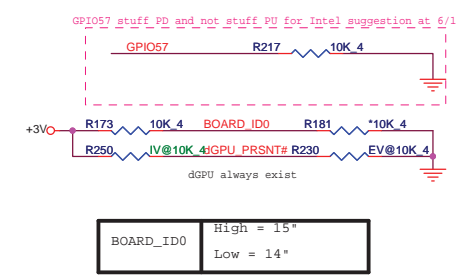
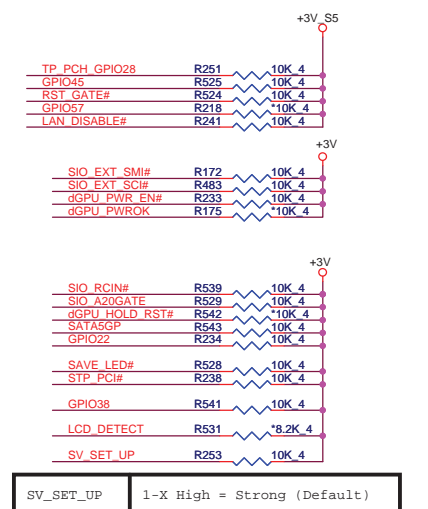
### IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)



### GPU\_RST#



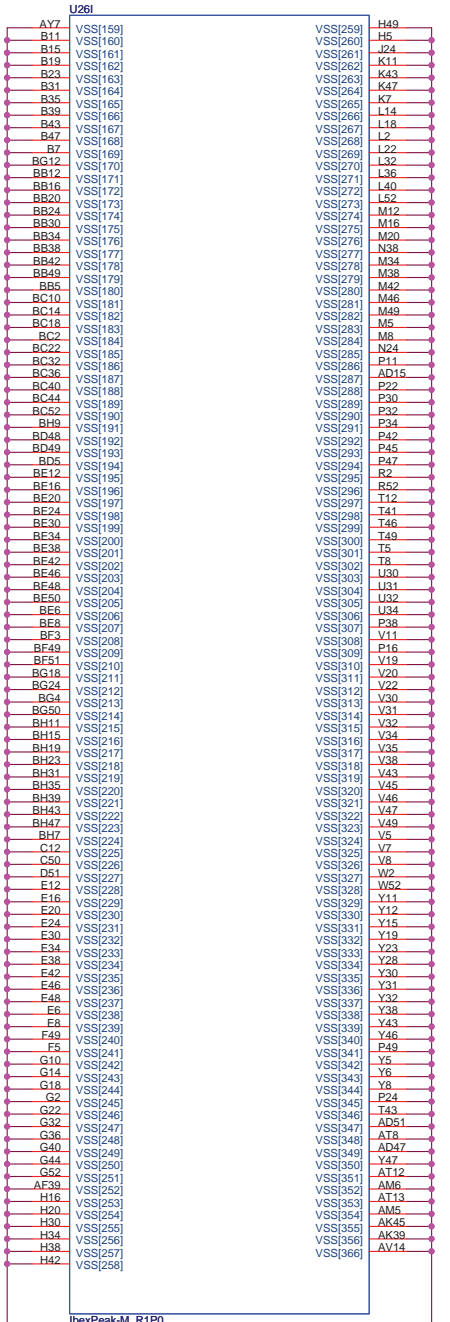
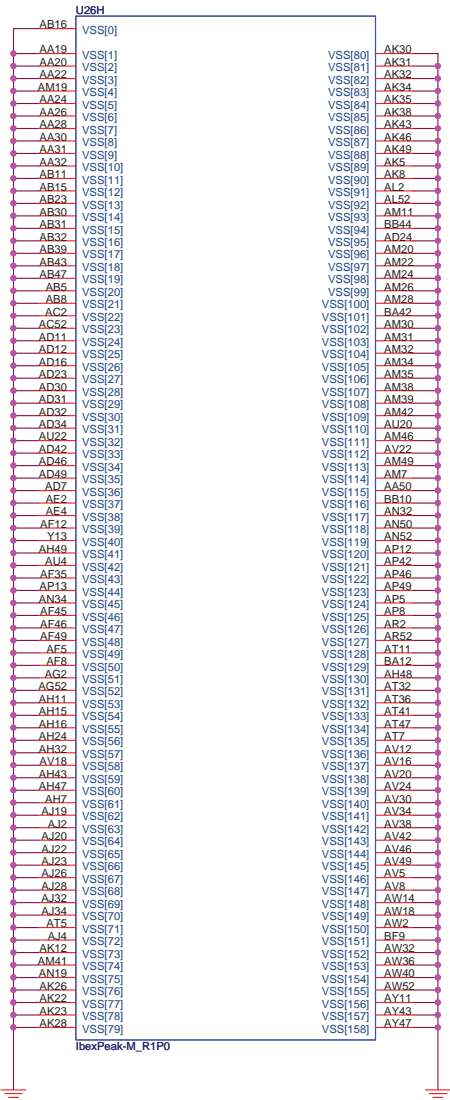
### GPIO Pull-up/Pull-down




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# IBEX PEAK-M (GND)

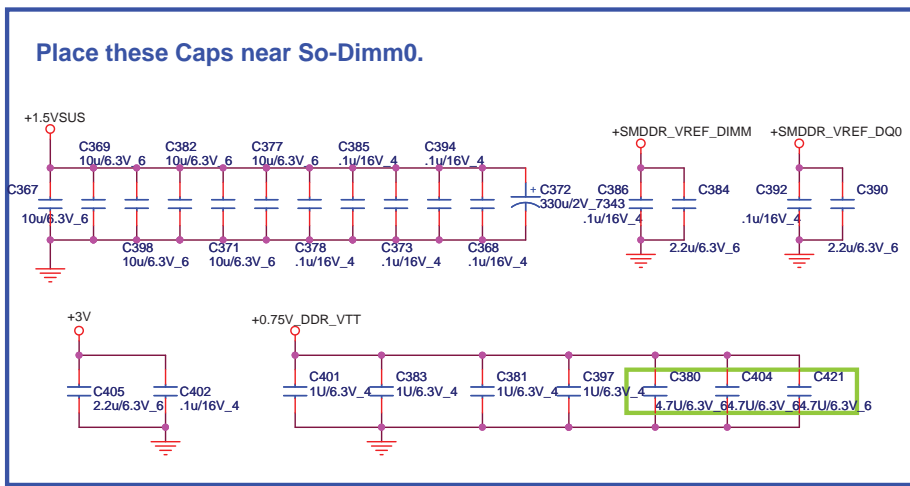
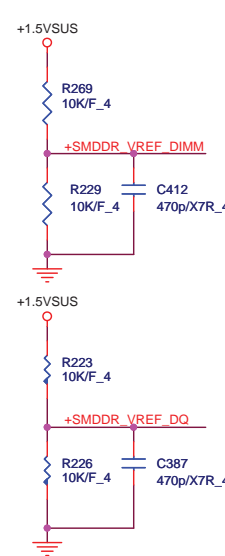
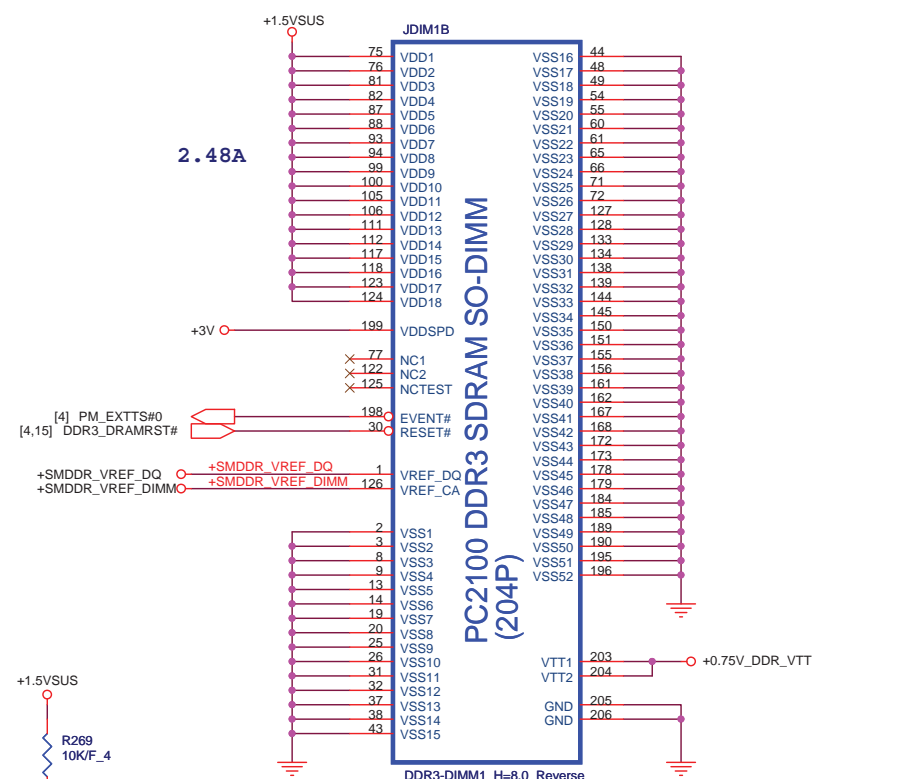
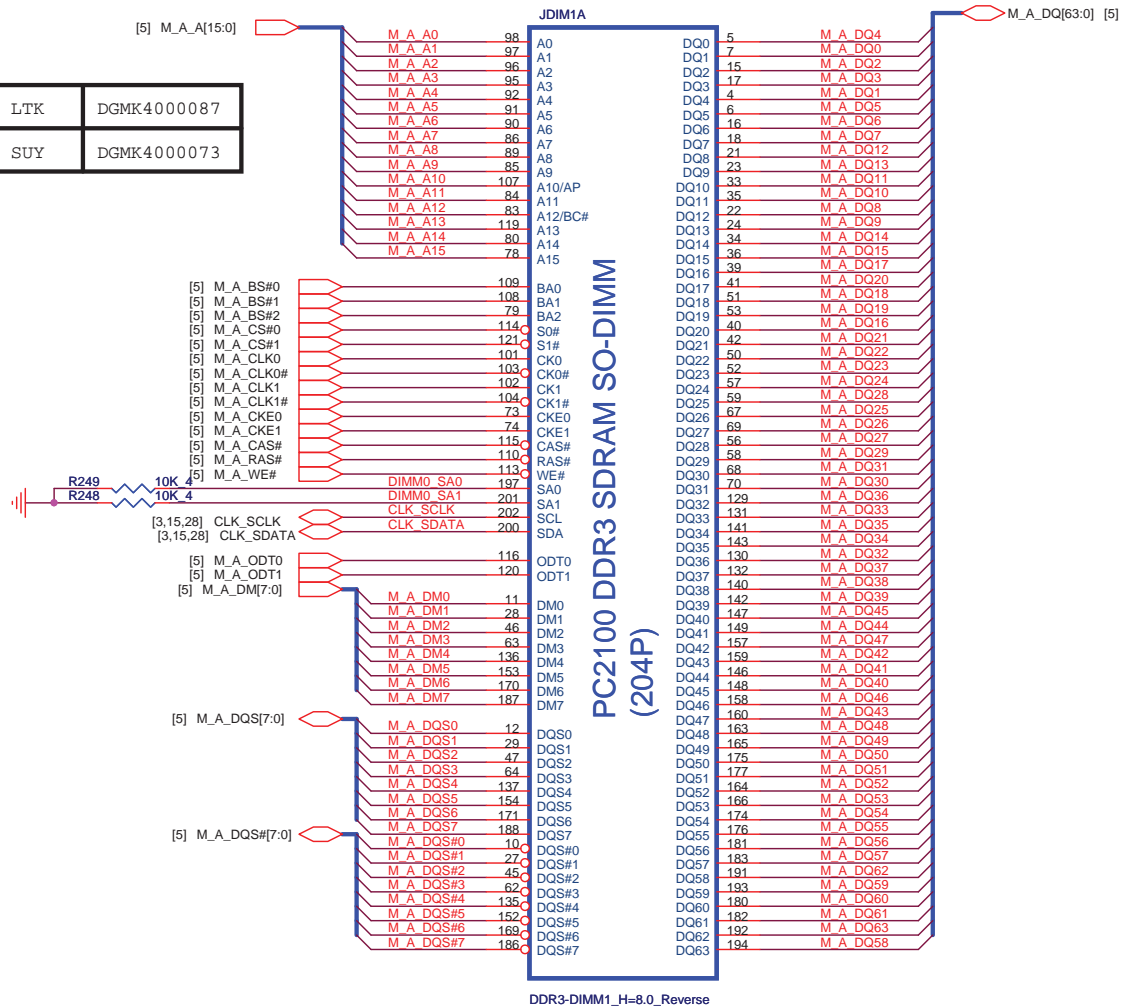




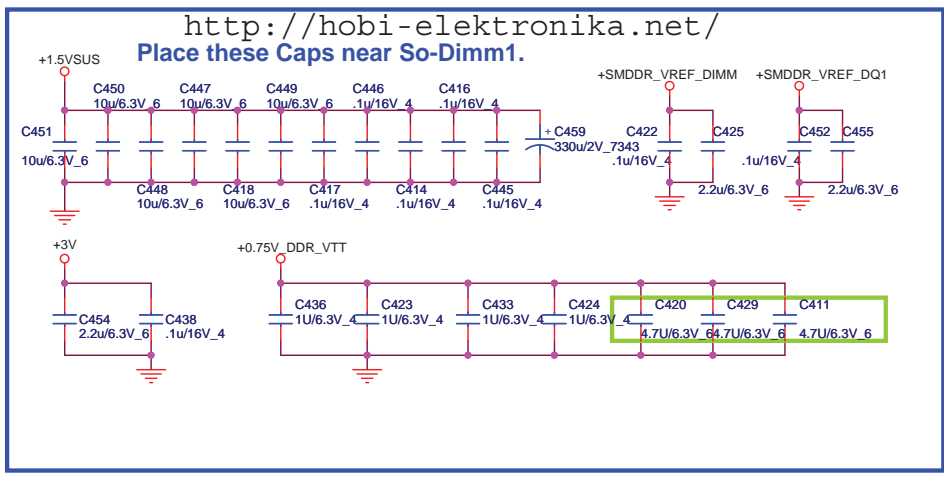
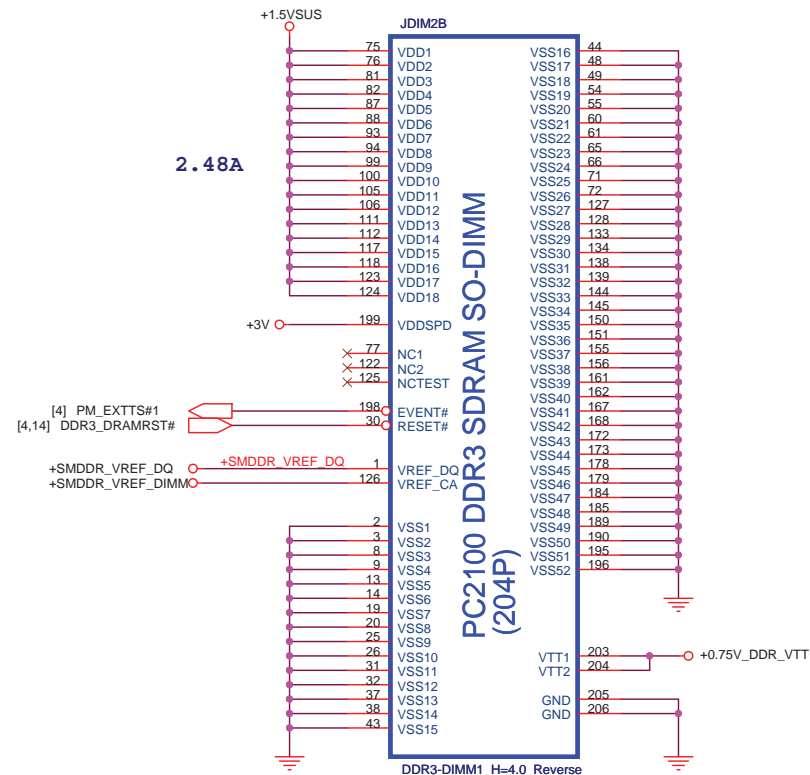
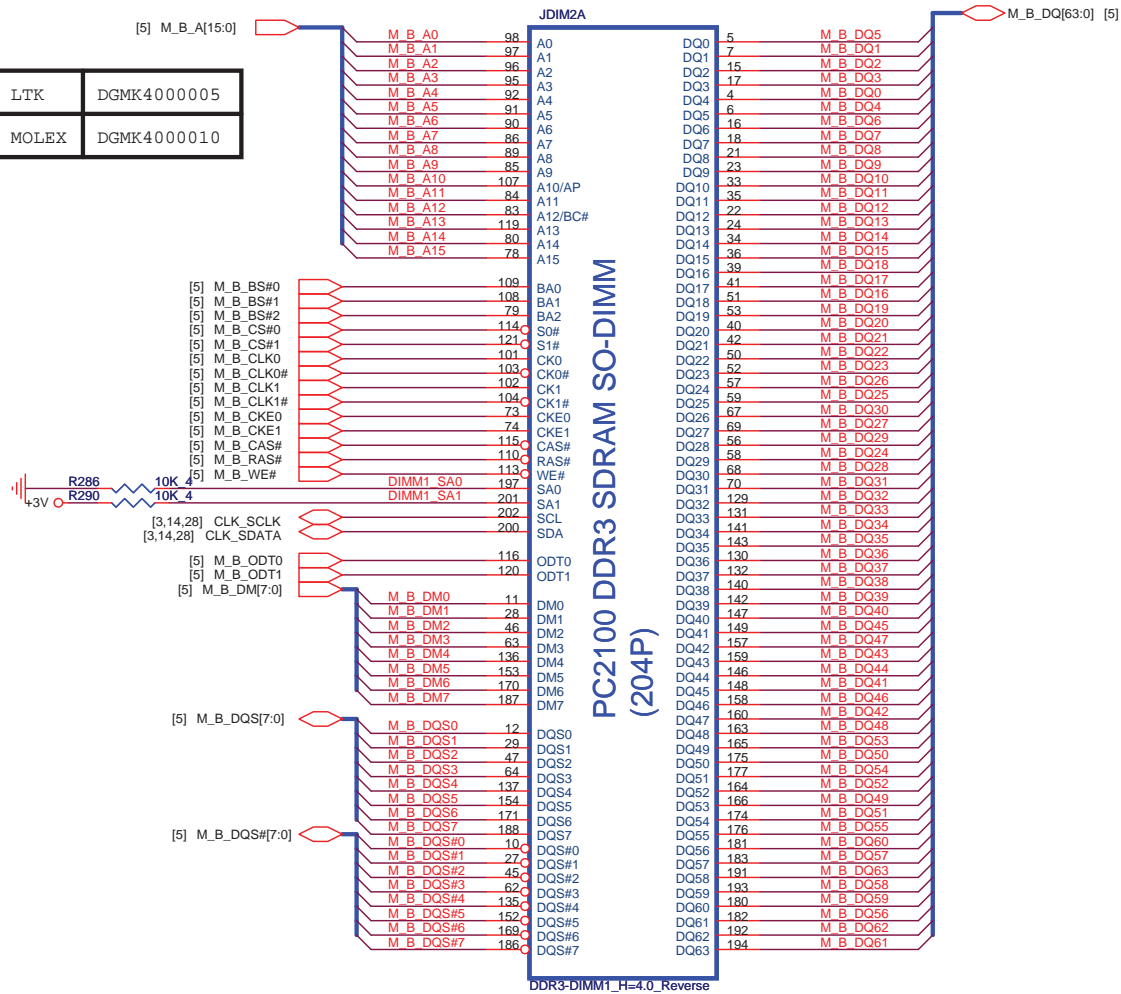
**Quanta Computer Inc.**  
PROJECT : ZRD

|       |                          |                |
|-------|--------------------------|----------------|
| Size  | Document Number          | Rev            |
|       | <b>IBEX PEAK-M 6/6</b>   | <b>1C</b>      |
| Date: | Wednesday, July 21, 2010 | Sheet 13 of 46 |

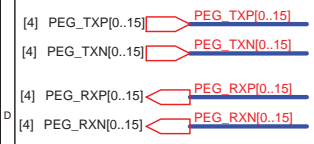
|     |             |
|-----|-------------|
| LTK | DGMK4000087 |
| SUY | DGMK4000073 |



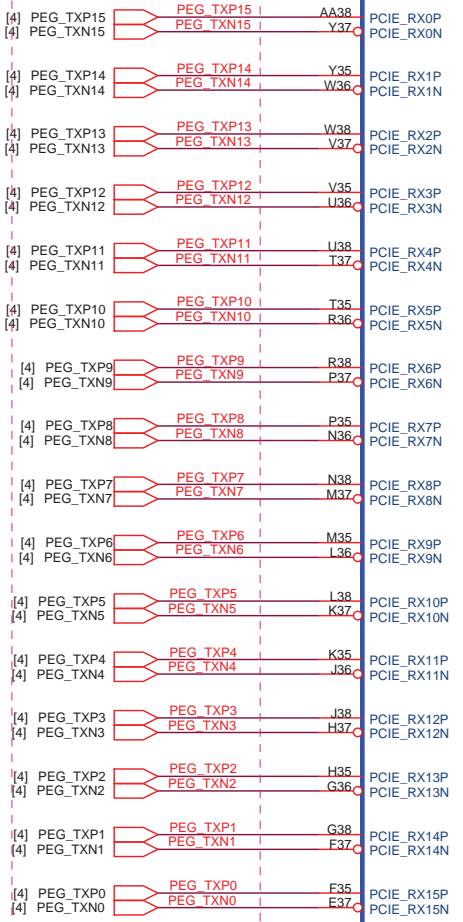
|       |             |
|-------|-------------|
| LTK   | DGMK4000005 |
| MOLEX | DGMK4000010 |



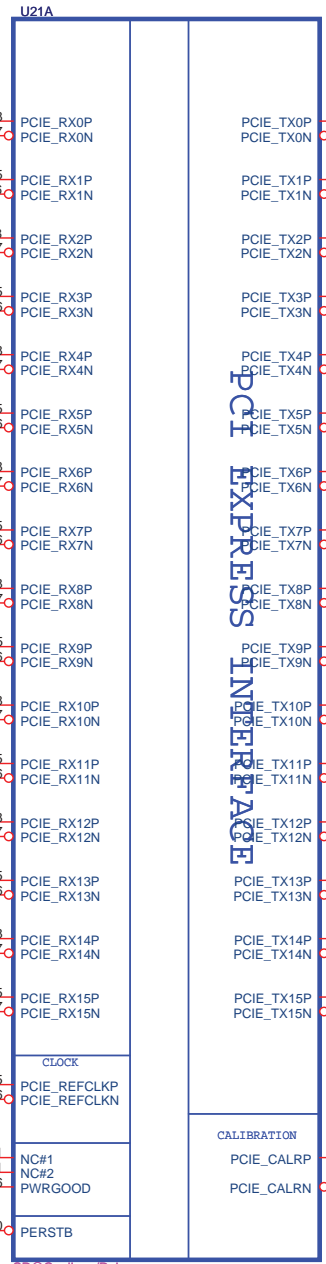
# GPU\_1(VGA)



0518 SWAP PCIE for VGA side



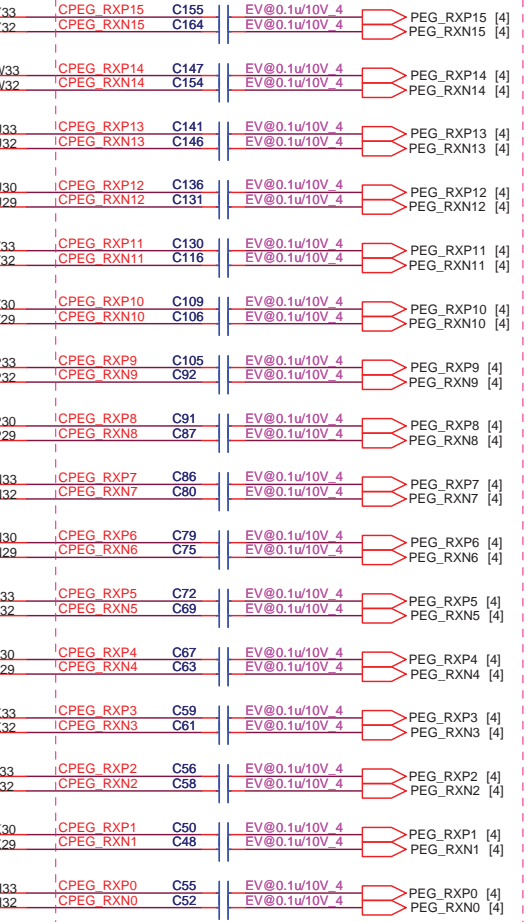
For Broadway, Madison and Park the PWRGOOD ball must be connected to ground



SP@Capilano/Robson

0518 SWAP PCIE for VGA side

PCI EXPRESS INTERFAC



For M97, Broadway, Madison and Park PCIE\_VDDC is 1.0V

|         |             |
|---------|-------------|
| Madison | AJ007720T02 |
| Park    | AJ077400T08 |

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|       |                                  |                |
|-------|----------------------------------|----------------|
| Size  | Document Number                  | Rev            |
|       | <b>Capilano/Robson -PCIE I/F</b> | 1C             |
| Date: | Wednesday, July 21, 2010         | Sheet 16 of 46 |

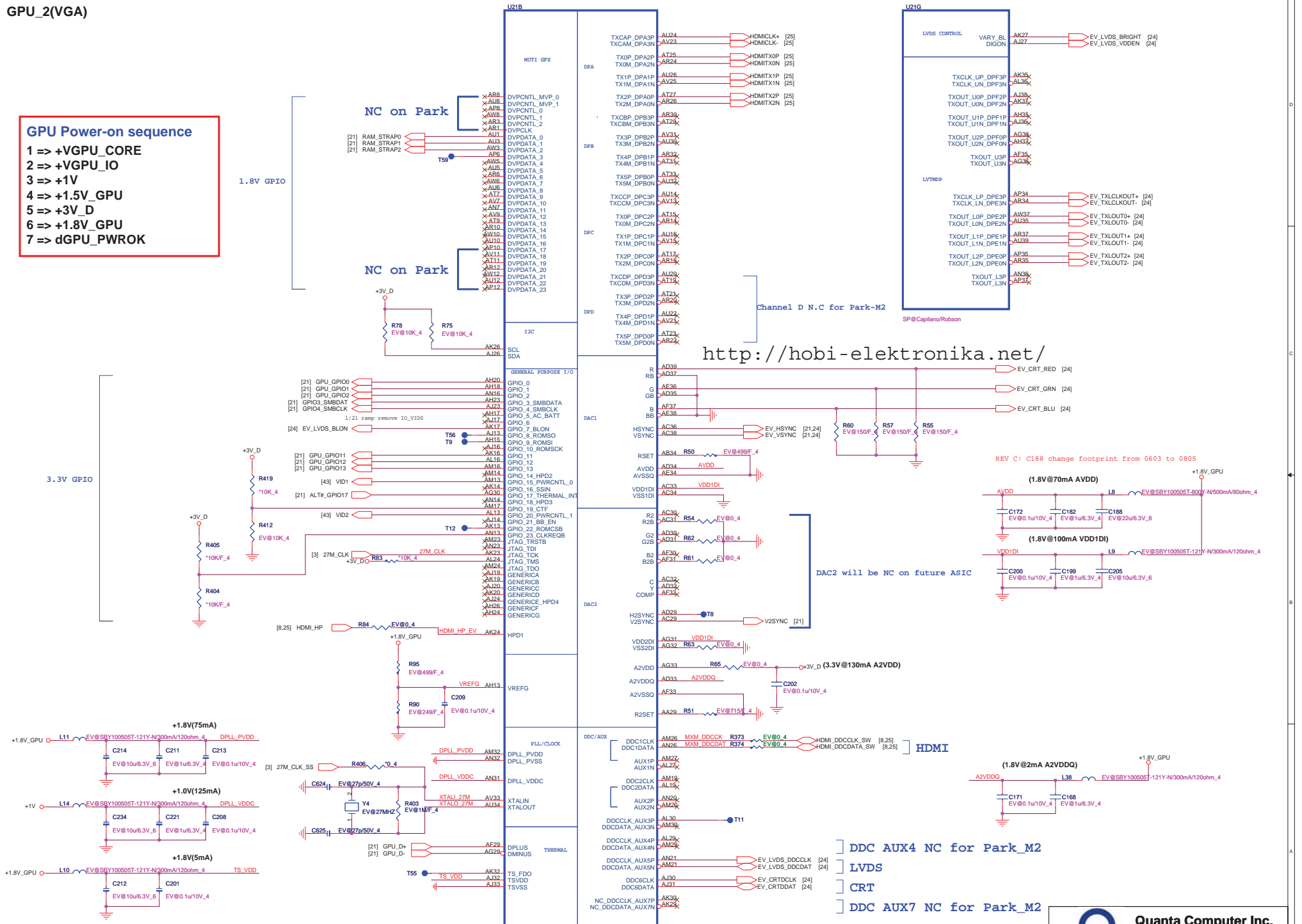


**GPU Power-on sequence**

- 1 => +VGPU\_CORE
- 2 => +VGPU\_IO
- 3 => +1V
- 4 => +1.5V\_GPU
- 5 => +3V\_D
- 6 => +1.8V\_GPU
- 7 => dGPU\_PWROK

1.8V GPIO

3.3V GPIO



<http://hobi-elektronika.net/>

REV C: C188 change footprint from 0603 to 0805

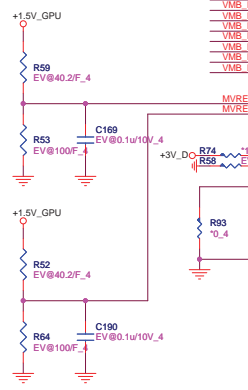
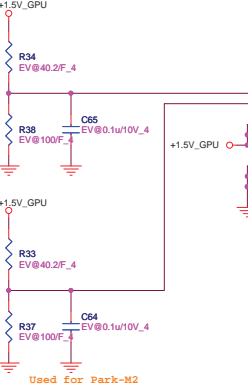
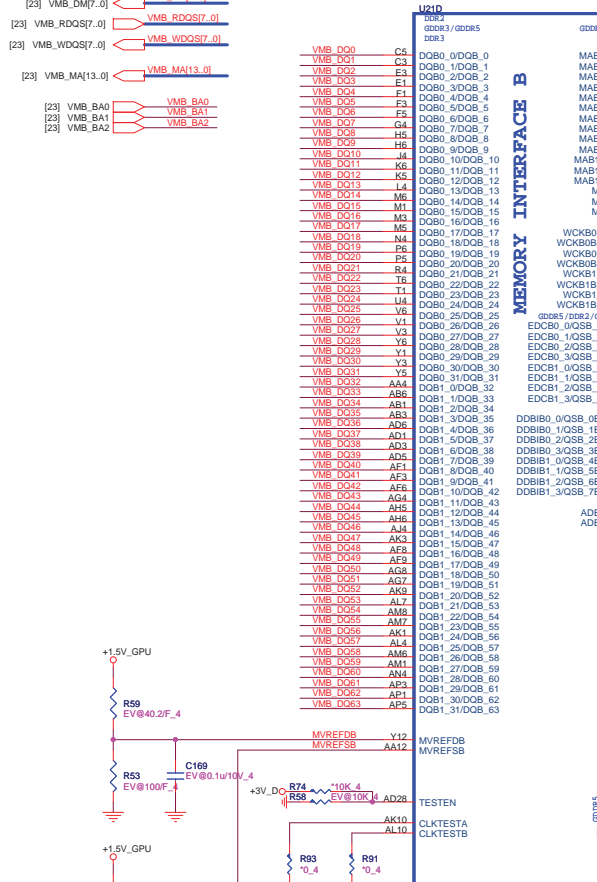
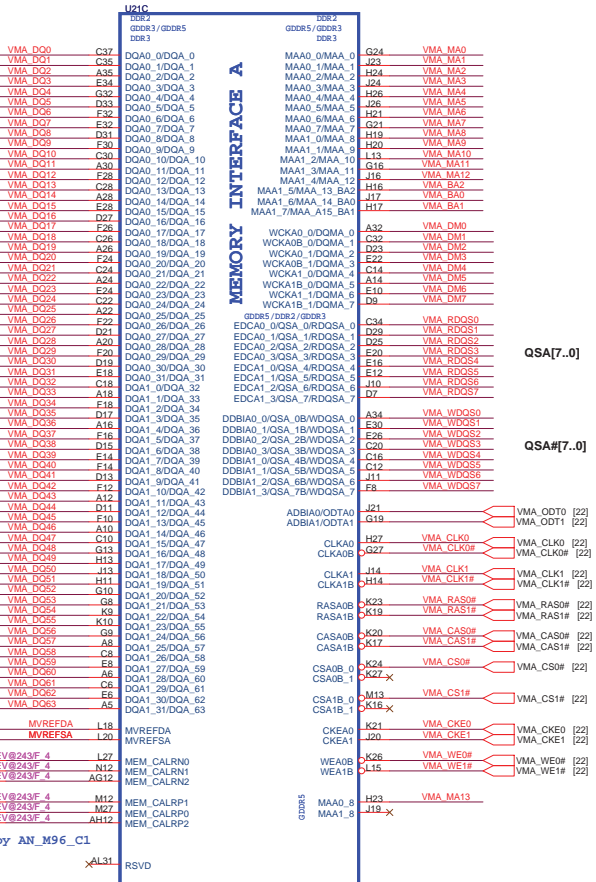
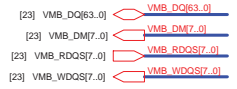
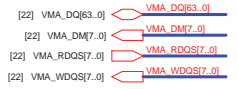
DAC2 will be NC on future ASIC

- ] DDC AUX4 NC for Park\_M2
- ] LVDS
- ] CRT
- ] DDC AUX7 NC for Park\_M2

SP@Caplano/Robson

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|       |                          |                |
|-------|--------------------------|----------------|
| Size  | Document Number          | Rev            |
|       | Caplano/Robson -PCIE I/F | 1C             |
| Date: | Wednesday, July 21, 2010 | Sheet 17 of 46 |



Used for Park-M2

Note by AN\_M96\_C1

SP@Caplano/Robson

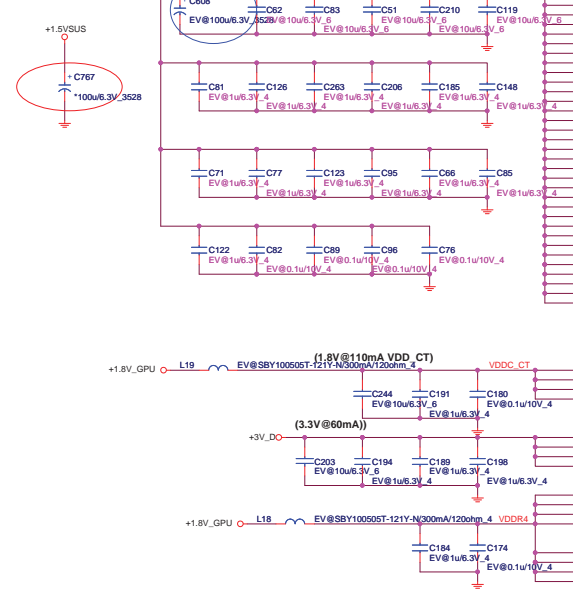
SP@Caplano/Robson

Place all these components very close to GPU

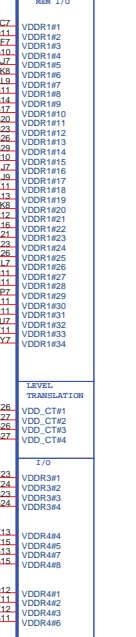
# GPU\_4(VGA)

For DDR3, MVDDQ = 1.5V (7.5A)

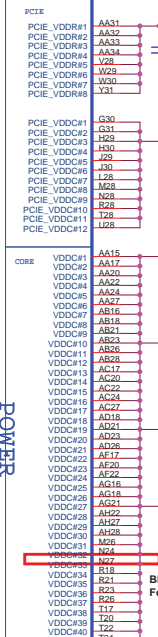
Near CN11, rev B add



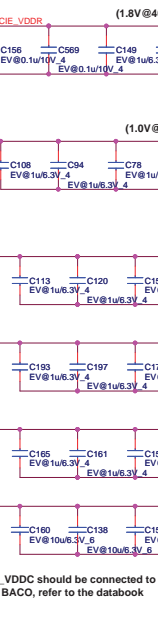
## POWER



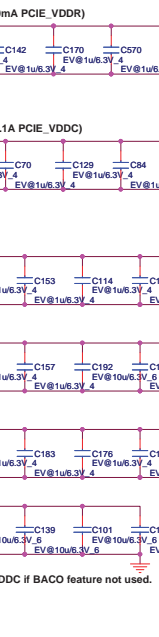
## PCIe



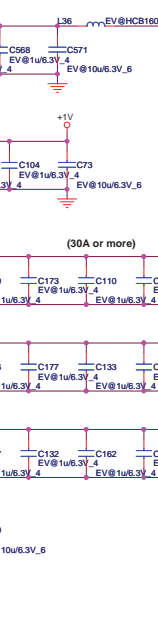
## CORE



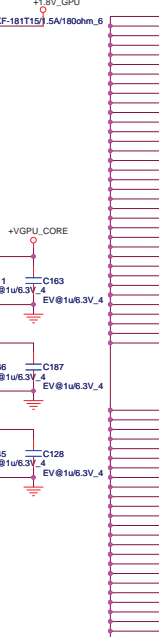
## VDDC CT



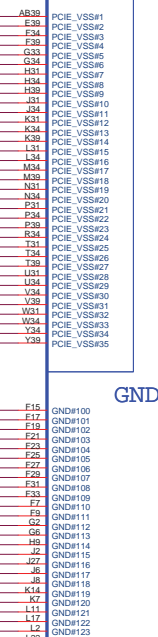
## VDD4



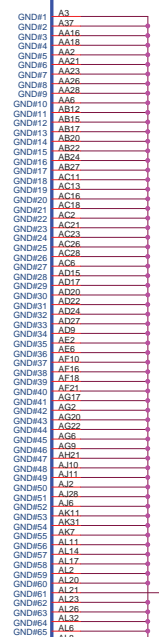
## MPV18



## SPV18



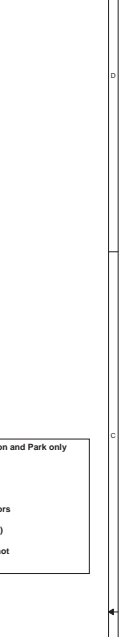
## FB\_VDDC



## GPU all PWROK



## GPU +3V power



BIF\_VDDC should be connected to VDDC if BACO feature not used. For BACO, refer to the databook

PIN different between Broadway and Madison

| Pin  | Broadway | Madison  |
|------|----------|----------|
| N27  | VDDC     | BIF_VDDC |
| AL31 | TS_A     | NC_TS_A  |
| AL21 | GND      | PX_EN    |

<http://hobi-elektronika.net/>

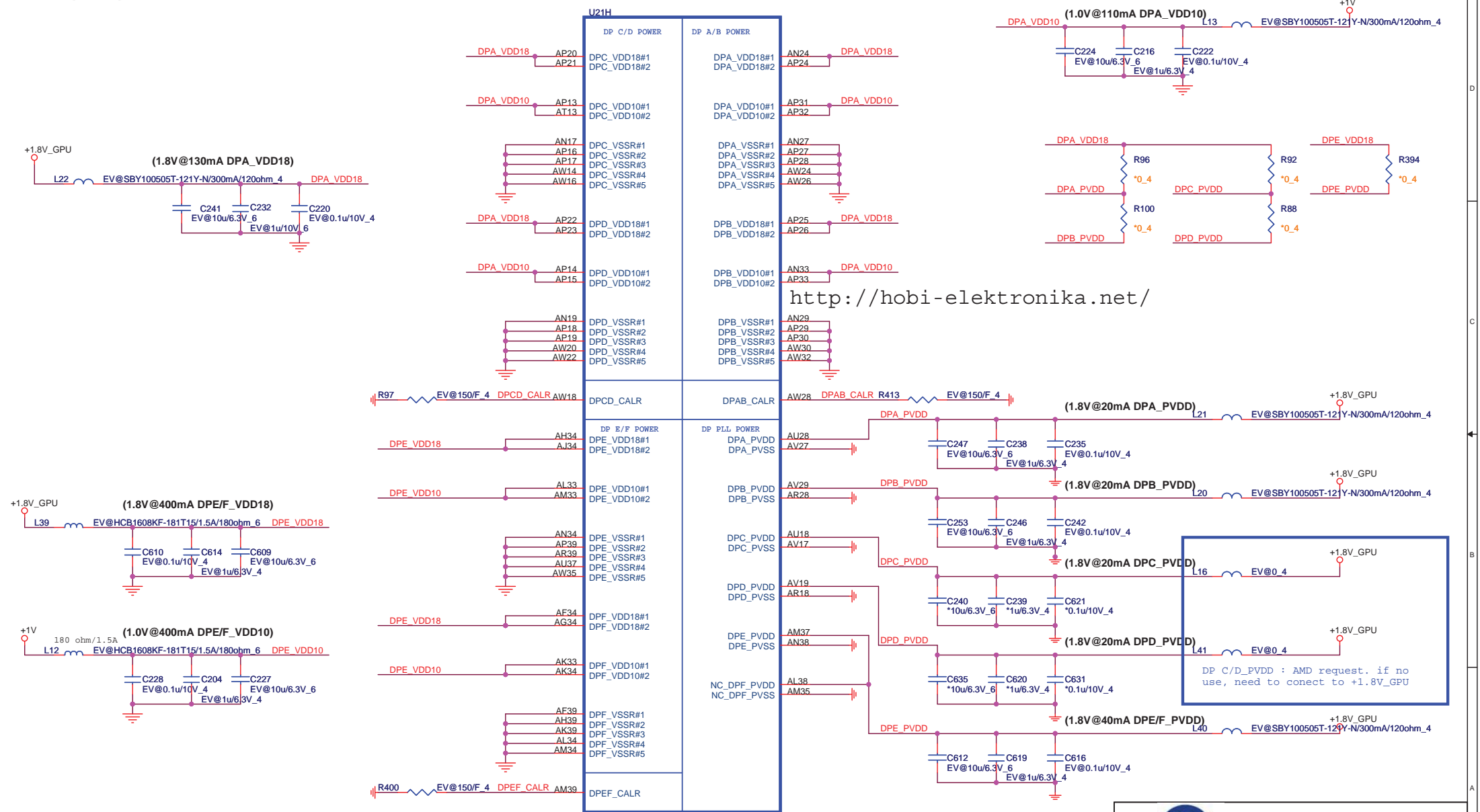
PowerXpress control signal for Madison and Park only  
 If not used, can be disconnected.  
 PX\_EN = LOW, turn on  
 PX\_EN = HIGH, turn off  
 PX\_EN is used to turn ON/OFF some regulators for PowerXpress mode. An output high 3.3V will turn the regulators OFF. An output low 0V will turn the regulators ON. PX\_EN outputs low (0V) by default.  
 If this signal is unused, it can be NC (not connected) or connected to ground.

Pin AL21 to Ground for Broadway

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PROJECT : ZRD


|                |                          |                |
|----------------|--------------------------|----------------|
| Size           | Document Number          | Rev            |
| Caplano/Robson | -PCIE I/F                | 1C             |
| Date:          | Wednesday, July 21, 2010 | Sheet 19 of 46 |

# GPU\_5(VGA)



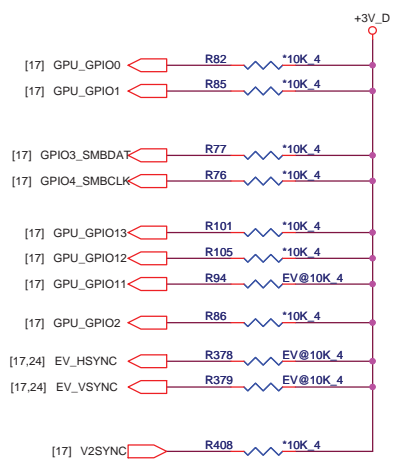
<http://hobi-elektronika.net/>

DP C/D\_PVDD : AMD request. if no use, need to connect to +1.8V\_GPU

|   |                          |       |                 |
|---|--------------------------|-------|-----------------|
|  <b>Quanta Computer Inc.</b><br>PROJECT :ZRD |                          | Rev   | 1C              |
|   |                          | Size  | Document Number |
| <b>Capilano/Robson -PCIE I/F</b>  |                          |       |                 |
| Date:   | Wednesday, July 21, 2010 | Sheet | 20 of 46        |

SP@Capilano/Robson

**PIN STRAPS(VGA)**



| Size of the primary memory apertures | GPIO[13:11]   |
|--------------------------------------|---------------|
| 128 MB                               | 000           |
| 256MB                                | 001           |
| 64 MB                                | 010           |
| 32 MB                                | 011           |
| More than 512 MB                     | Not Supported |

| CONFIGURATION STRAPS  |                           |   |         |                 |
|---|---------------------------|---|---------|-----------------|
| ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET |                           |   |         |                 |
| STRAPS  | PIN                       | DESCRIPTION OF DEFAULT SETTINGS   | DEFAULT | REMARK          |
| TX_PWRS_ENB   | GPIO0                     | 0 = 50% TX OUTPUT SWING<br>1 = FULL TX OUTPUT SWING   | 0       |                 |
| TX_DEEMPH_EN  | GPIO1                     | PCIE TRANSMITTER DE-EMPHASIS ENABLED<br>0 = TX DE-EMPHASIS DISABLED<br>1 = TX DE-EMPHASIS ENABLED   | 0       |                 |
| BIOS_ROM_EN   | GPIO_22_ROMCSB            | Enable external BIOS ROM device<br>0 - Disable external BIOS ROM device<br>1 - Enable external BIOS ROM device  | 0       |                 |
| ROMIDCFG[2:0]   | GPIO[13:11]               | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT  | 001     | See ROM table   |
| BIF_GEN2_EN_A   | GPIO2                     | 0 = PCIE DEVICE AS 2.5GT/S CAPABLE<br>1 = PCIE DEVICE AS 5GT/S CAPABLE  | 0       |                 |
| GPIO_8_ROMSO<br>H2SYNC<br>GPIO_21_BB_EN   | GPIO8<br>H2SYNC<br>GPIO21 | Reserved Only   | 0       |                 |
| AUD[1]<br>AUD[0]  | HSYNC<br>VSYNC            | AUD[1:0]<br>00: NO AUDIO FUNCTION.<br>01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED.<br>10: AUDIO FOR DISPLAYPORT ONLY.<br>11: AUDIO FOR BOTH DISPLAYPORT AND HDMI. | 11      | See Audio table |
| GPIO_9_ROMSI  | GPIO9                     | 0 = VGA controller capacity enable  | 0       |                 |
| VIP_DEVICE_STRAP_ENA  | V2SYNC                    | 0 = DRIVER would ignore the value sample on VHAD_0 during RESET.  | 0       |                 |

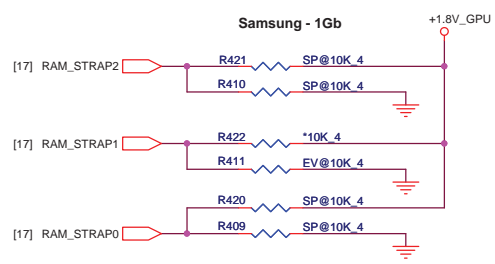
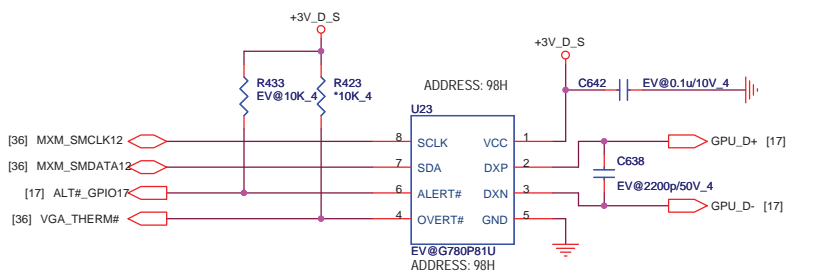
**DDR3 Memory Aperture size(GPU)**

| DDR3 Memory size |                 |                       |                         |                         |                         |
|------------------|-----------------|-----------------------|-------------------------|-------------------------|-------------------------|
| Vendor           | Vendor P/N      | STN B/S P/N           | RAM_STRAP2<br>DVPDATA_2 | RAM_STRAP1<br>DVPDATA_1 | RAM_STRAP0<br>DVPDATA_0 |
| Hynix            |                 |                       | 1                       | 1                       | 0                       |
|                  | H5TQ1G63BFR-12C | AKD5LZGTW04 (64M*16)  | 1                       | 0                       | 0                       |
|                  | H5TQ2G63BFR-12C | AKD5MGGTW03 (128M*16) | 1                       | 0                       | 1                       |
| Samsung          |                 |                       |                         |                         |                         |
|                  | K4W1G1646E-HC12 | AKD5LGGT506 (64M*16)  | 0                       | 0                       | 0                       |
|                  | K4W2G1646B-HC12 | AKD5MGGT500 (128m*16) | 0                       | 0                       | 1                       |
| AMD              |                 |                       |                         |                         |                         |
|                  | 23EY2387MA12-SZ | AKD5LGGT700           | 0                       | 1                       | 0                       |

**Thermal Sensor(VGA)**

| Vendor   | P/N         |
|----------|-------------|
| WINDBOND | AL83L771K01 |
| GMT      | AL000780000 |

USD0.16



RAM\_STRAP2 SET DDR3 Vendor  
RAM\_STRAP[1:0] SET SIZE.

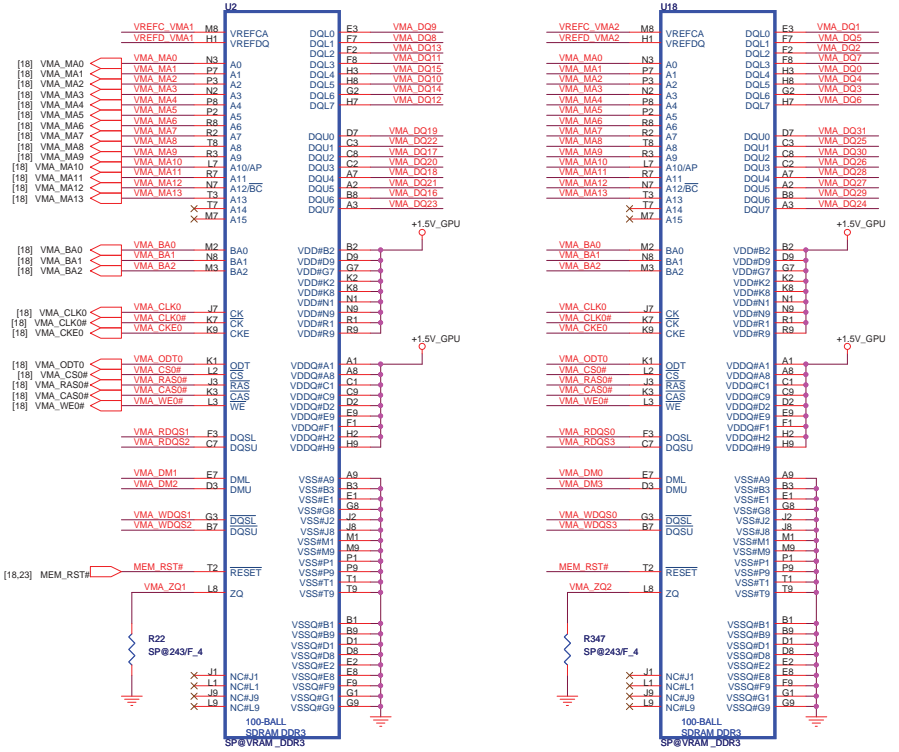
**Quanta Computer Inc.**  
PROJECT :ZRD

Size Document Number Strip/Thermal Rev 1C  
Date: Wednesday, July 21, 2010 Sheet 21 of 46

# CHANNEL A: 512MB DDR3 (64M\*16\*4pcs)

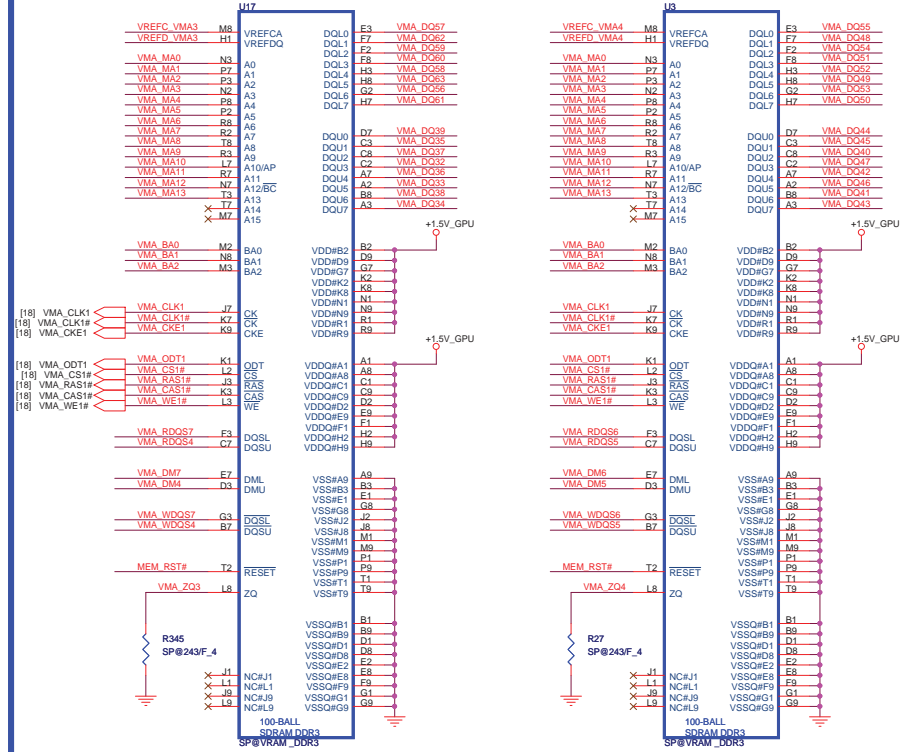
- [18] VMA\_DQ[63..0] VMA\_DQ[63..0]
- [18] VMA\_DM[7..0] VMA\_DM[7..0]
- [18] VMA\_RDQS[7..0] VMA\_RDQS[7..0]
- [18] VMA\_WDQS[7..0] VMA\_WDQS[7..0]

QSA[7..0]  
QSA#[7..0]



TOP Left

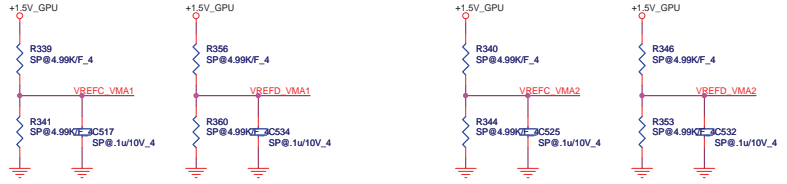
BOT Left



BOT Right

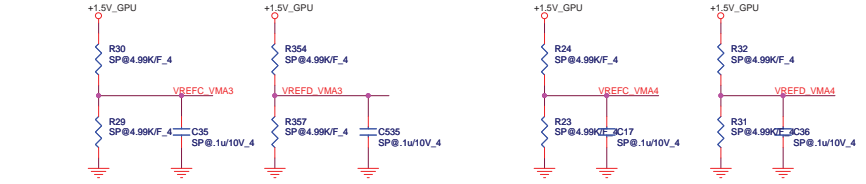
TOP Right

## Group-A0 VREF

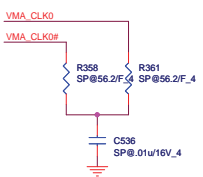


## Group-A1 VREF

<http://hobi-elektronika.net/>

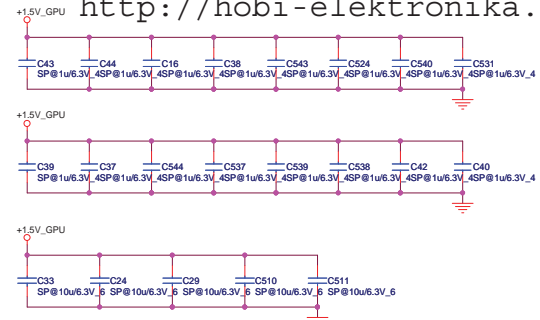


## MEM\_A0 CLK



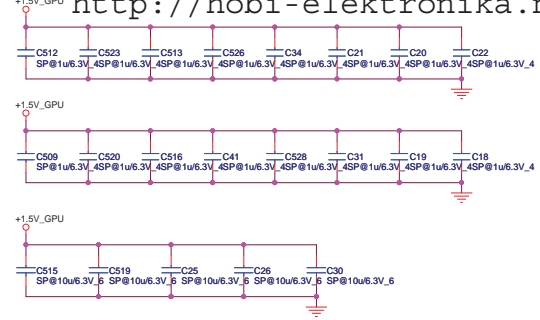
## Group-A0 decoupling CAP

<http://hobi-elektronika.net/>

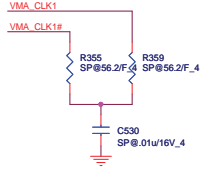


## Group-A1 decoupling CAP

<http://hobi-elektronika.net/>



## MEM\_A1 CLK

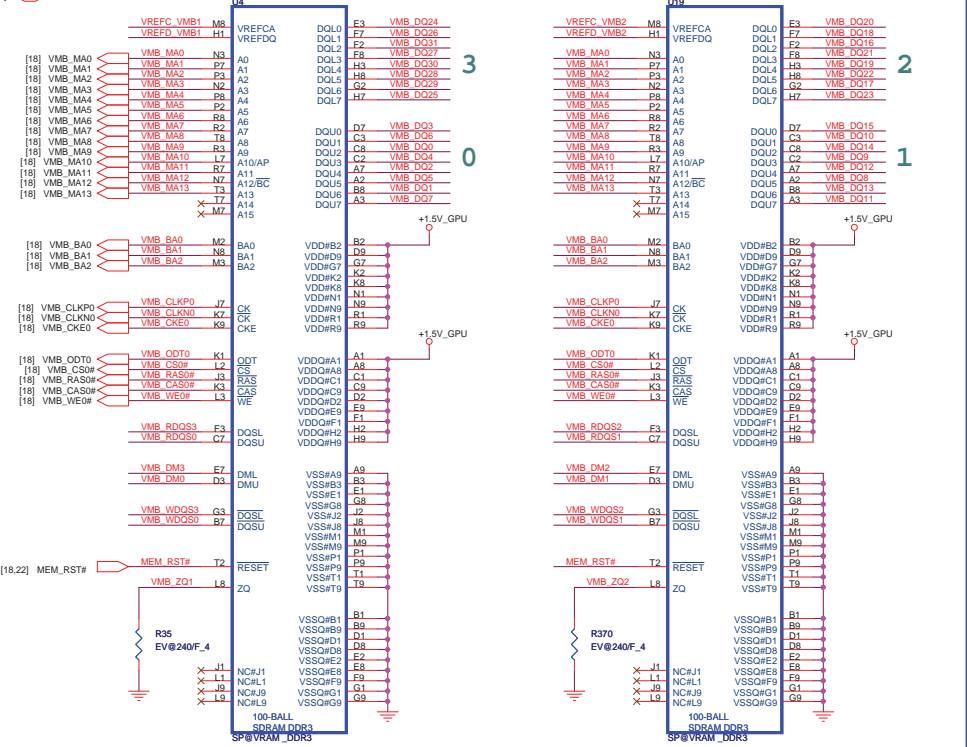


# CHANNEL B: 512MB DDR3 (16\*64M\*4pcs)

Park, M92M Use Channel B Memory Interface Only

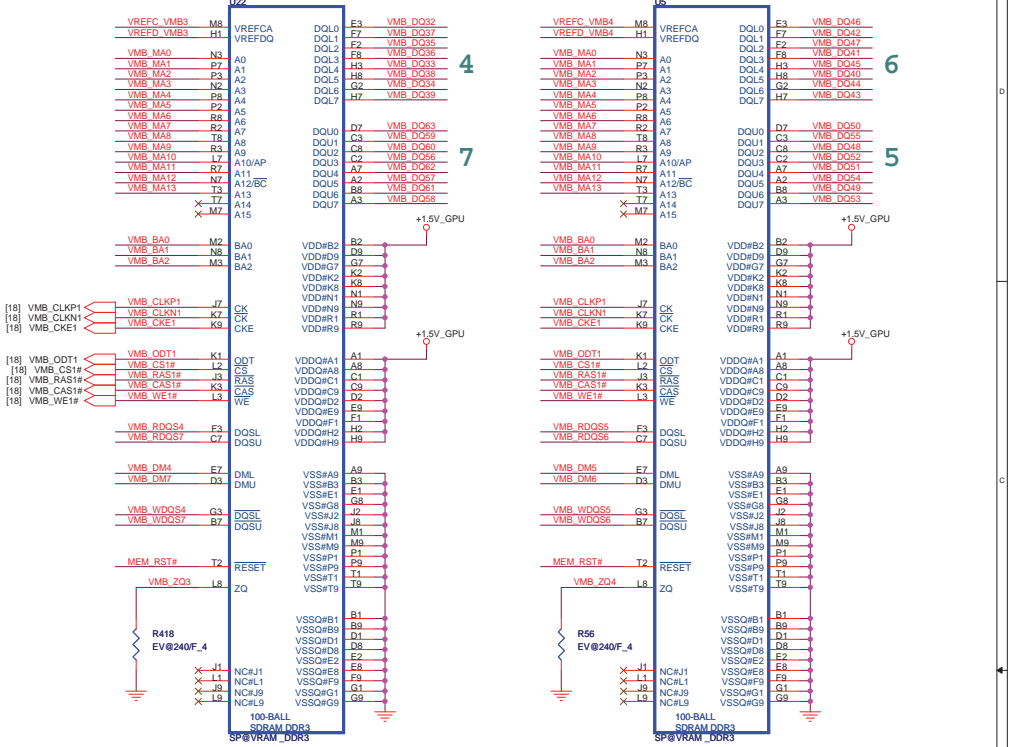
- [18] VMB\_DM[63..0] VMB\_DM63\_0
- [18] VMB\_DM[7..0] VMB\_DM7\_0
- [18] VMB\_RDQS[7..0] VMB\_RDQS7\_0
- [18] VMB\_WDQS[7..0] VMB\_WDQS7\_0

QSA#7..0  
QSA#7..0



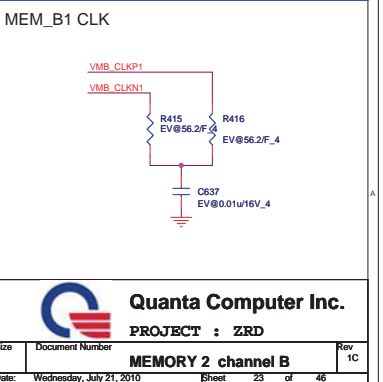
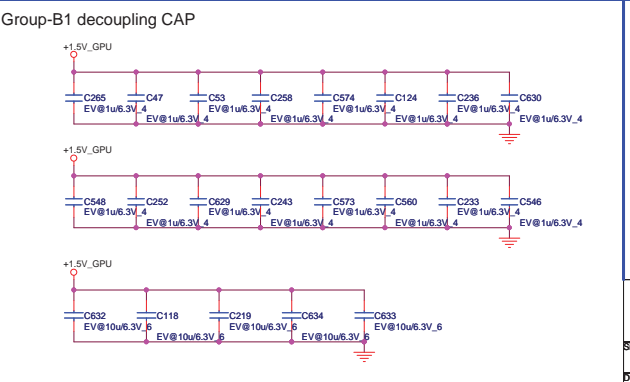
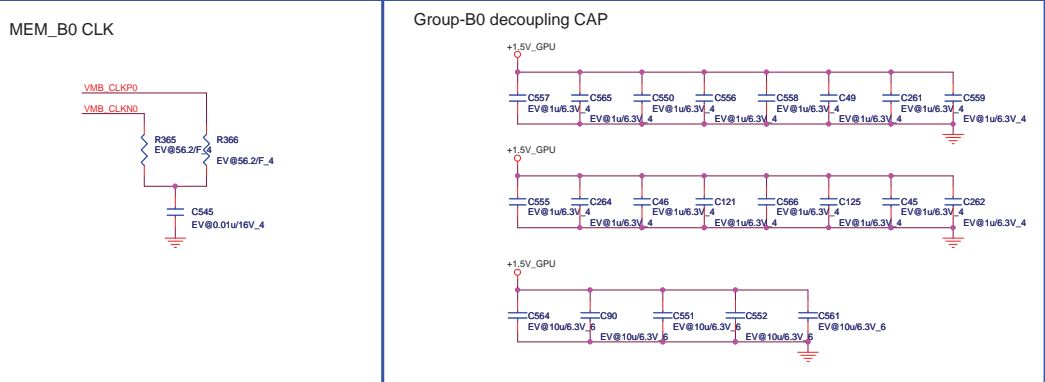
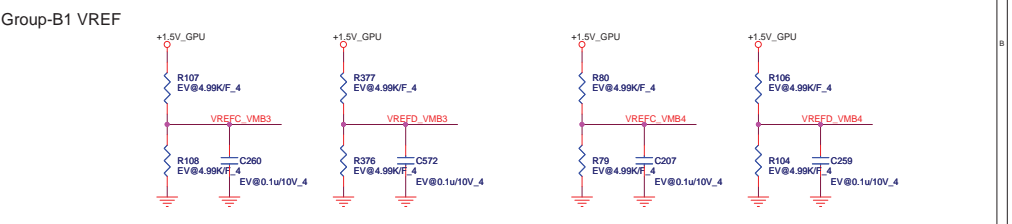
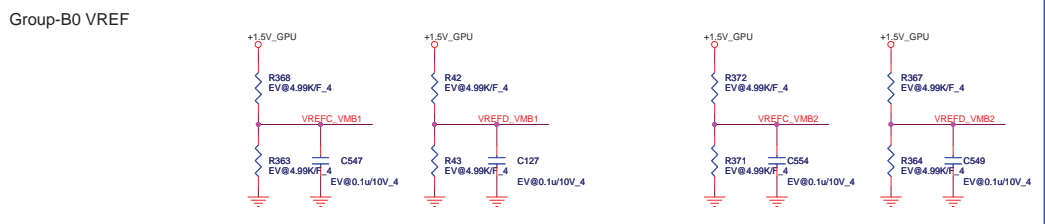
BOT Down

TOP Down



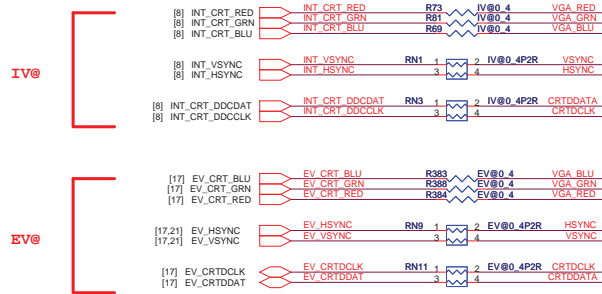
TOP Up

BOT Up

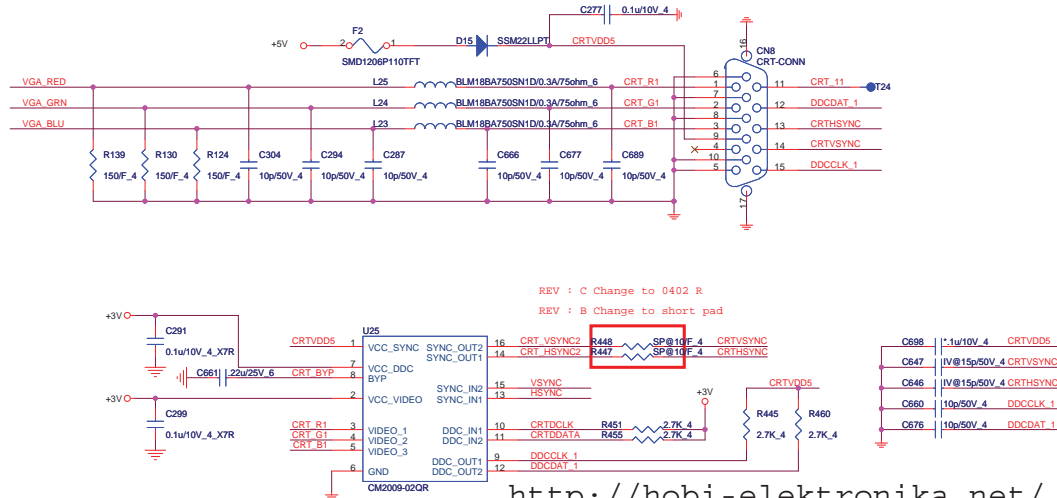


# CRT Switch

0\_ohm Resistor place close to Joint-Point



# CRT

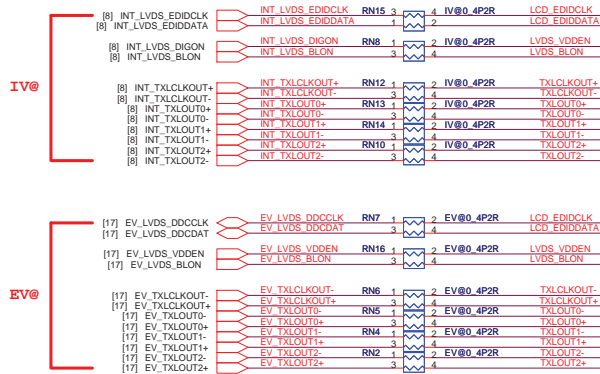


REV : C Change to 0402 R  
REV : B Change to short pad

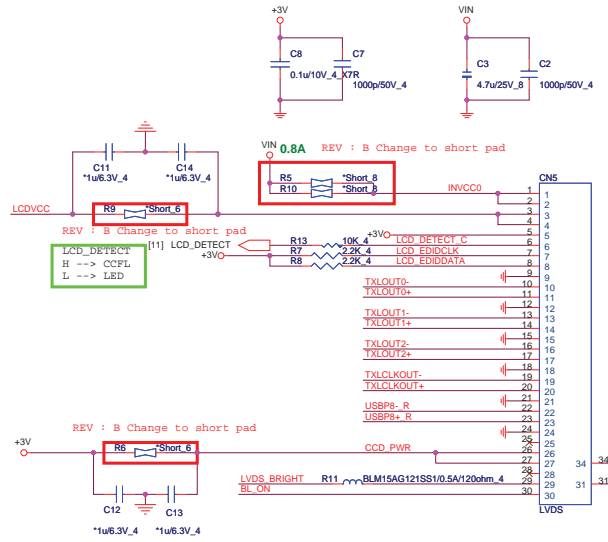
<http://hobi-elektronika.net/>

# LVDS

0\_ohm Resistor place close to Joint-Point



# LVDS

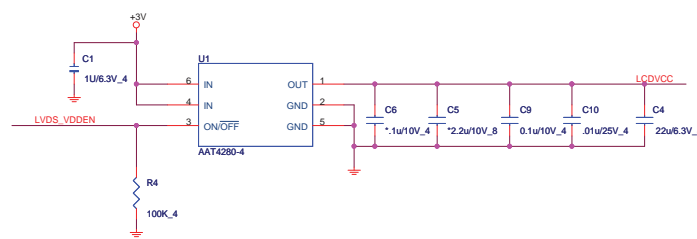


REV : B Change to short pad

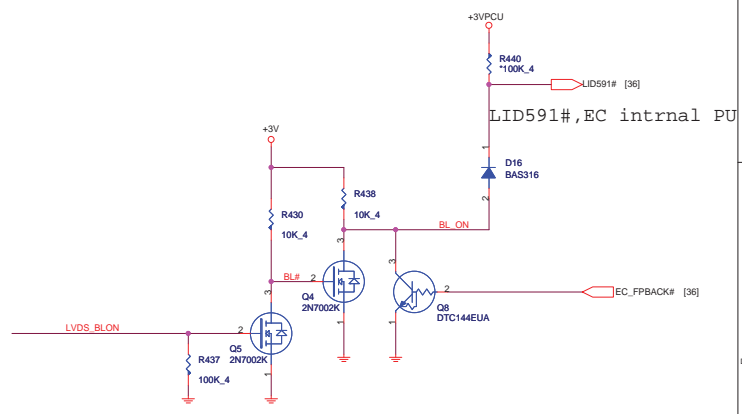
REV : B Change to short pad

<http://hobi-elektronika.net/>

# LCD Power



Backlight Control <http://hobi-elektronika.net/>



# LVDS\_BRIGHT

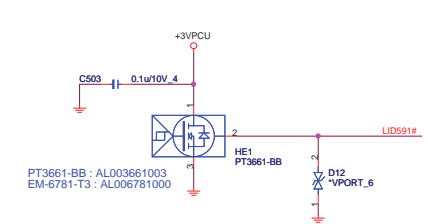


# CCD-USB



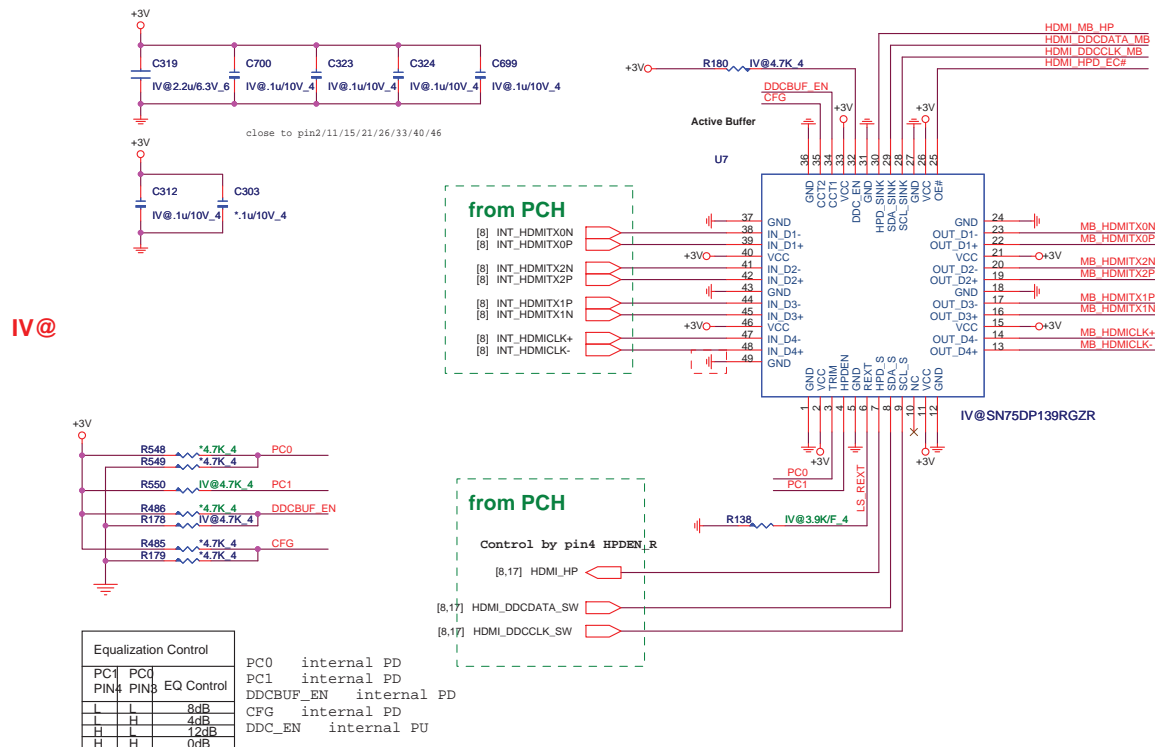
CCD +3V-current budget 0.2A

# Lid Switch (Hall sensor)



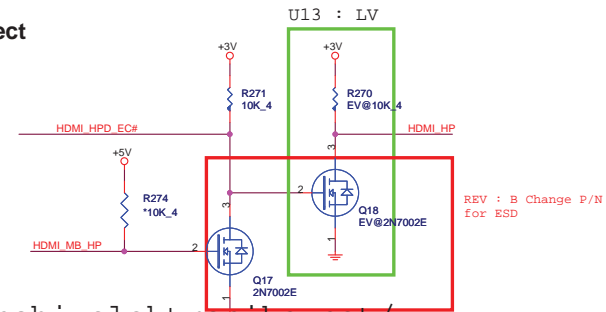


# HDMI LEVEL SHIFTER



# HDMI-detect

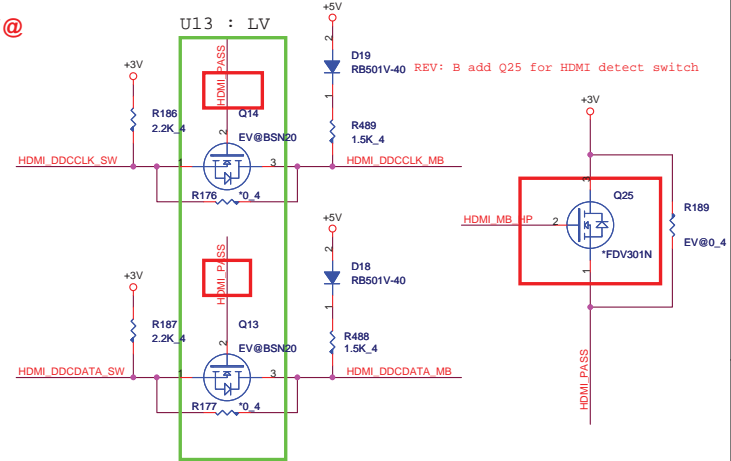
EV@



<http://hobi-elektronika.net/>

# I2C

EV@

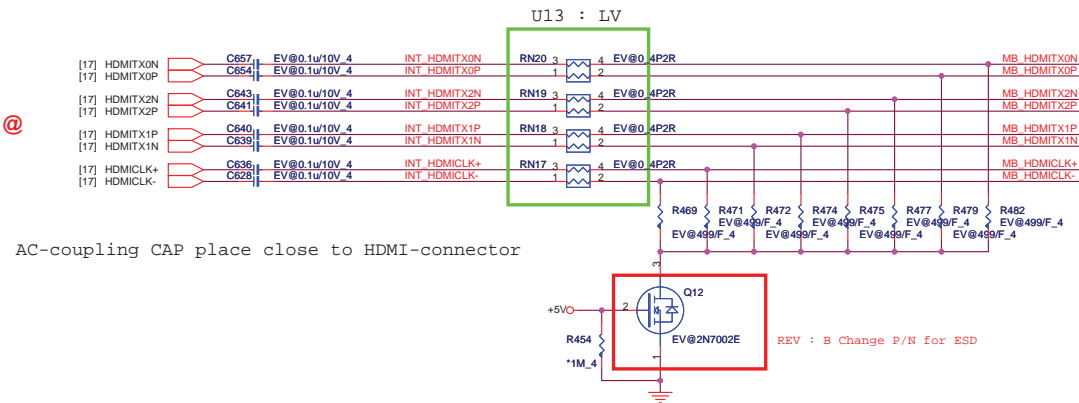


<http://hobi-elektronika.net/>

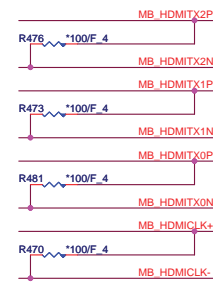
# Switchable Graphic HDMI source

<http://hobi-elektronika.net/>

EV@

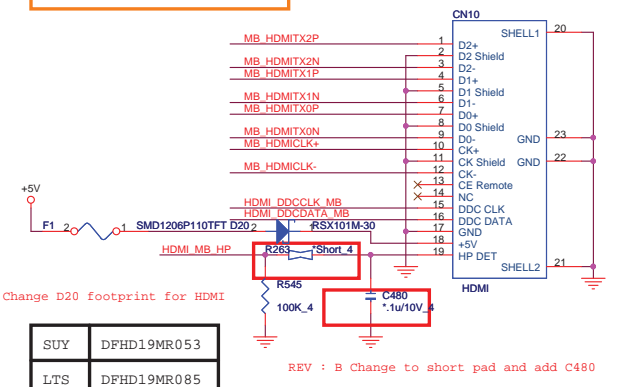


# EMI

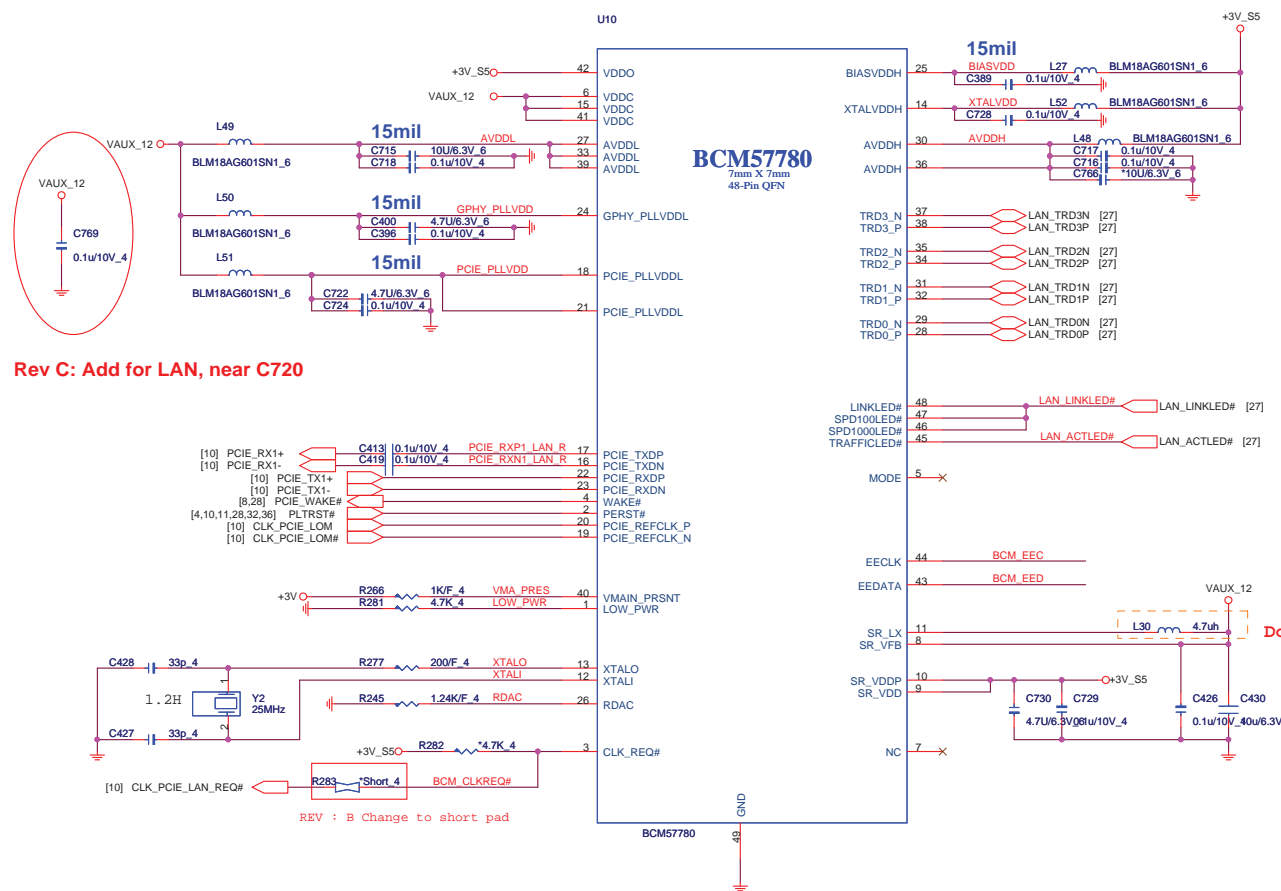


# HDMI connector

REV : C Location :D20 Change Footprint & P/N

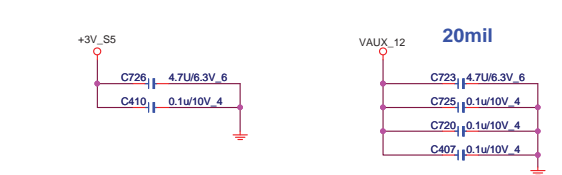


# Giga-LAN BCM57780

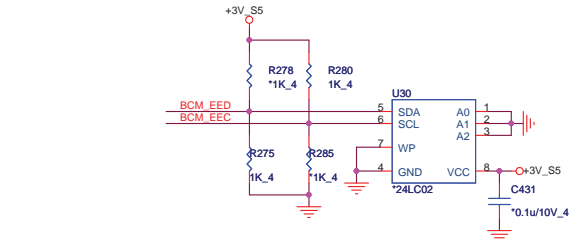


Rev C: Add for LAN, near C720

## LAN POWER



## EEPROM

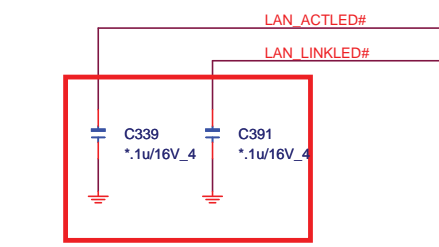
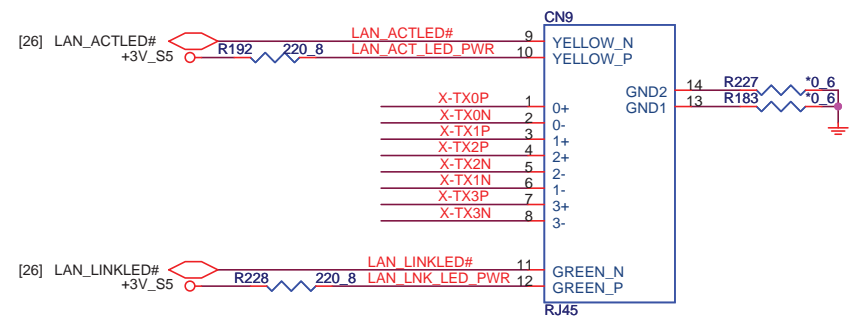
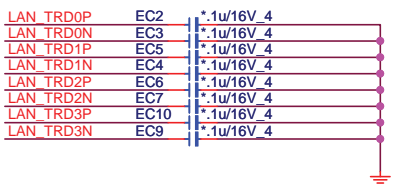
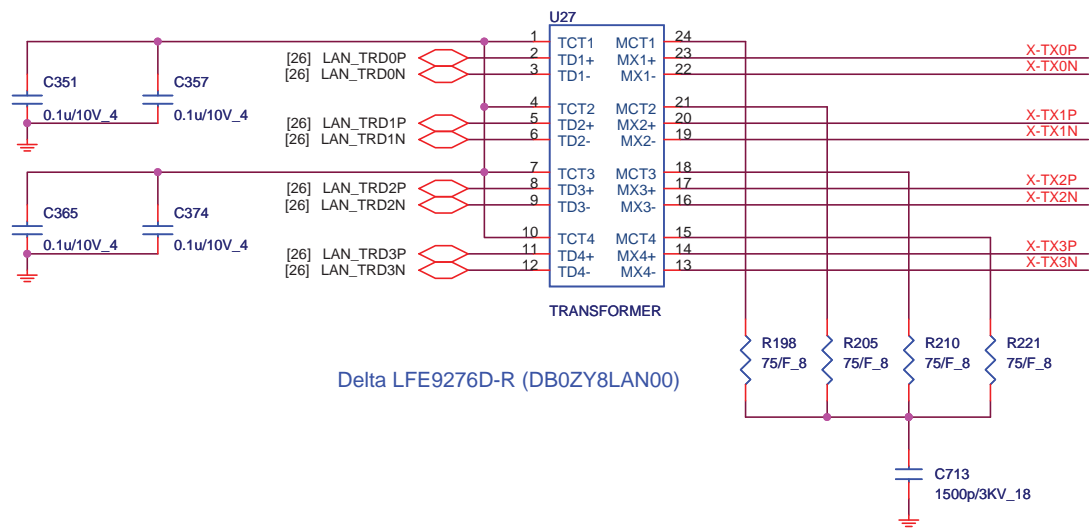


### EEPROM Strapping


| EEPROM Type | EECLK | EEDATA |
|-------------|-------|--------|
| 24LC02      | 1     | 1      |
| Internal    | 1     | 0      |

# TRANSFORMER

|     |             |
|-----|-------------|
| SUY | DFTJ12FR109 |
| AEC | DFTJ12FR135 |



REV : B Change to 0402 for ESD



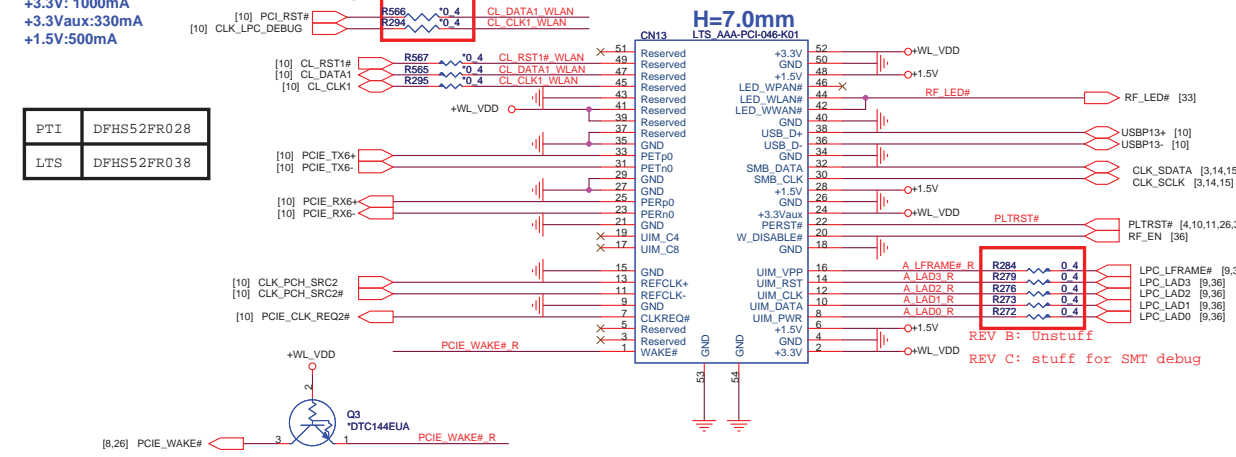
**Quanta Computer Inc.**  
PROJECT : ZRD

|       |                                 |                |
|-------|---------------------------------|----------------|
| Size  | Document Number                 | Rev            |
|       | <b>LAN Transformer and RJ45</b> | 1C             |
| Date: | Wednesday, July 21, 2010        | Sheet 27 of 46 |

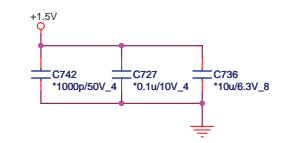
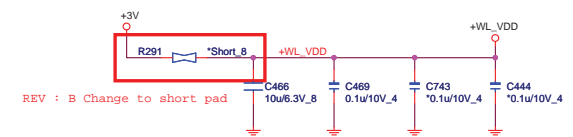
# MINI-CARD WLAN(MPC)

+3.3V: 1000mA  
 +3.3Vaux: 330mA  
 +1.5V: 500mA

REV : B Unstuff  
 Debug



|     |             |
|-----|-------------|
| PTI | DFHS52FR028 |
| LTS | DFHS52FR038 |



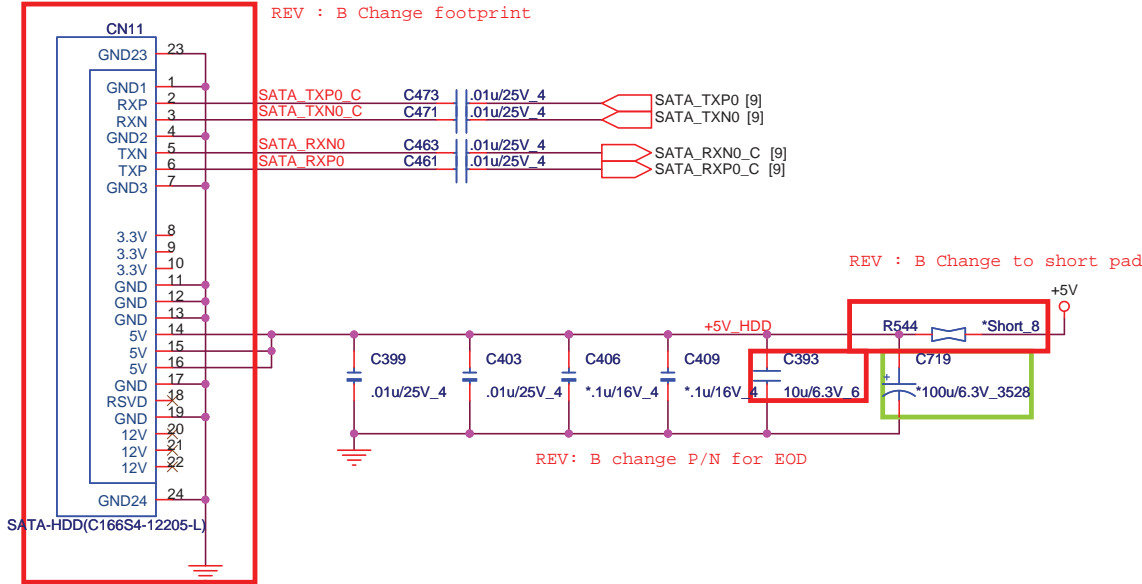
**Quanta Computer Inc.**  
 PROJECT : ZRD

|      |                 |     |
|------|-----------------|-----|
| Size | Document Number | Rev |
|      |                 | 1C  |

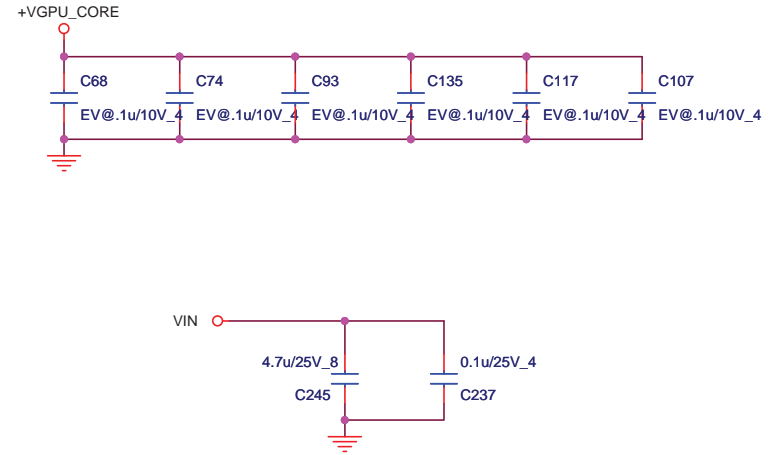
Date: Wednesday, July 21, 2010 Sheet 28 of 46

# MAIN SATA HDD

REV : B Change footprint

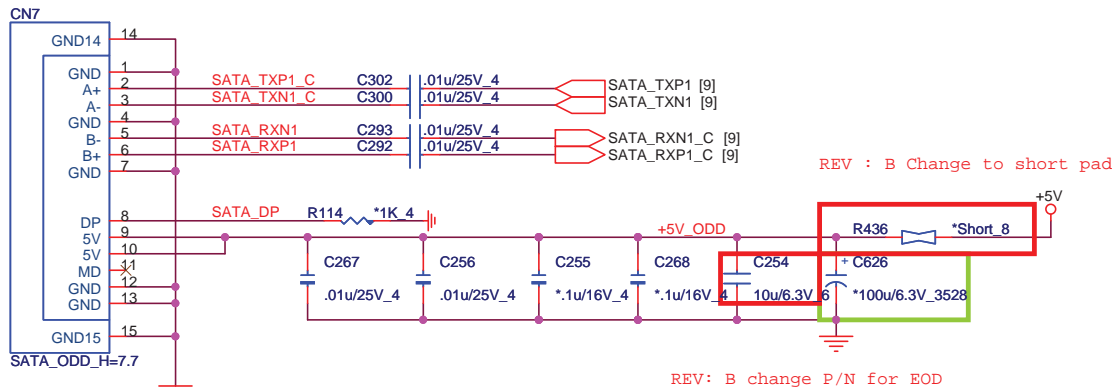


# EE RETURN-PATH CAPACITORS



# ODD (SATA)

<http://hobi-elektronika.net/>



|     |             |
|-----|-------------|
| SUY | DFHS22FR214 |
| AOP | DFHS22FR232 |
| AEC | DFHS22FR216 |

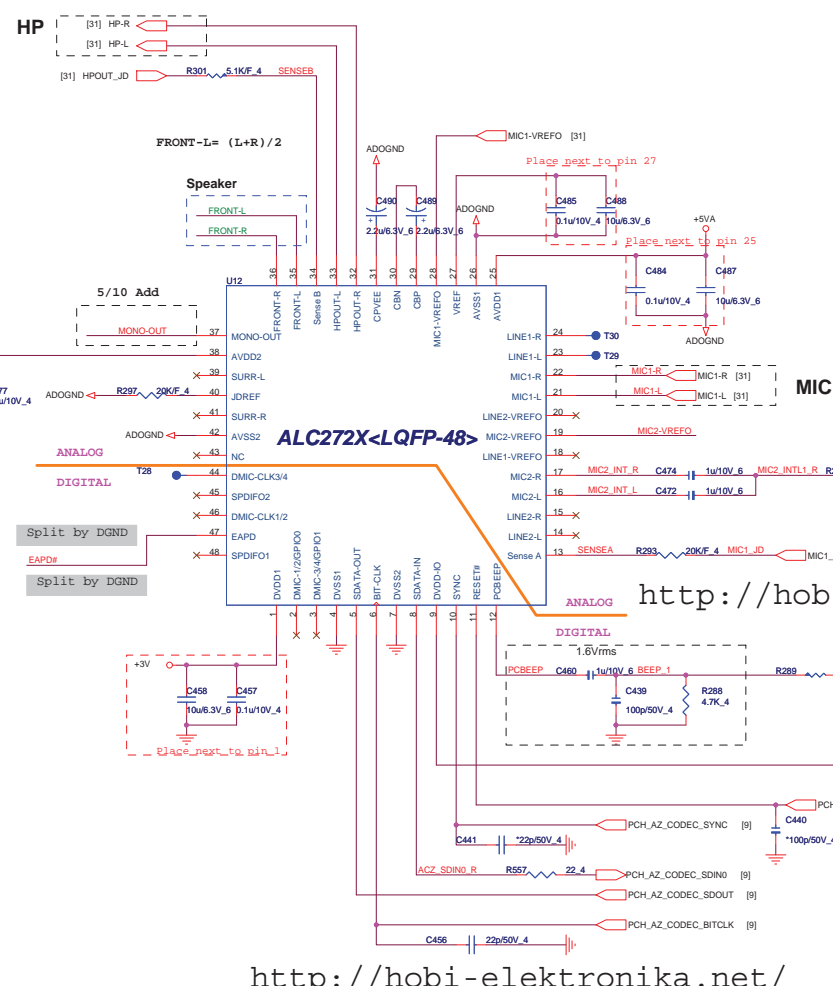
|     |             |
|-----|-------------|
| AOP | DFHS13FR011 |
| OTK | DFHS13FR010 |

**Quanta Computer Inc.**

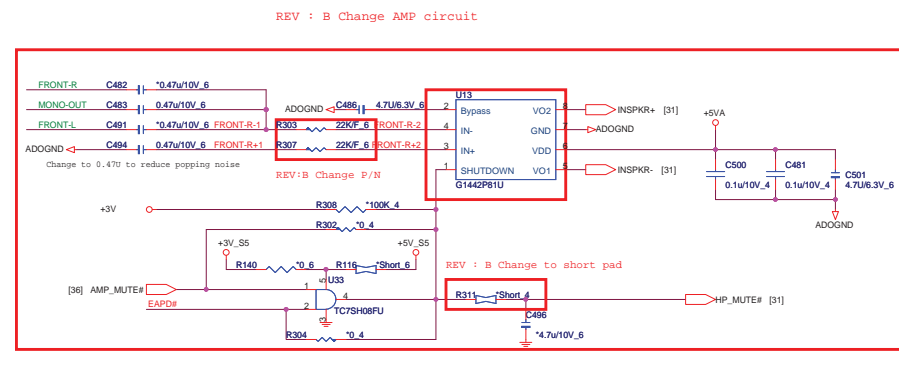
**PROJECT : ZRD**

|       |                                 |                |
|-------|---------------------------------|----------------|
| Size  | Document Number                 | Rev            |
|       | <b>SATA-HDD/ODD/RETURN-PATH</b> | <b>1C</b>      |
| Date: | Wednesday, July 21, 2010        | Sheet 29 of 46 |

**Codec(ADO)**



**MUTE(AMP)**



<http://hobi-elektronika.net/>

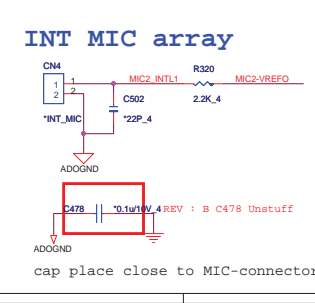
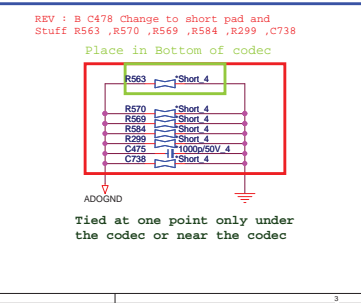
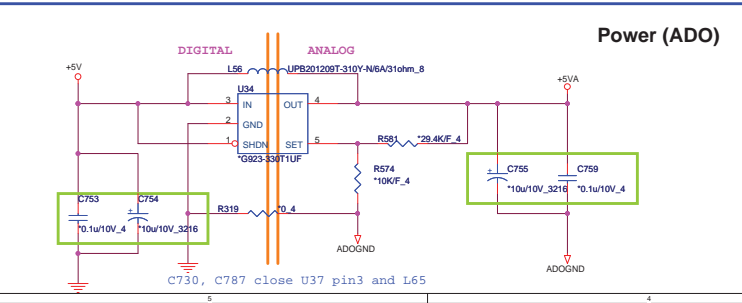
<http://hobi-elektronika.net/>

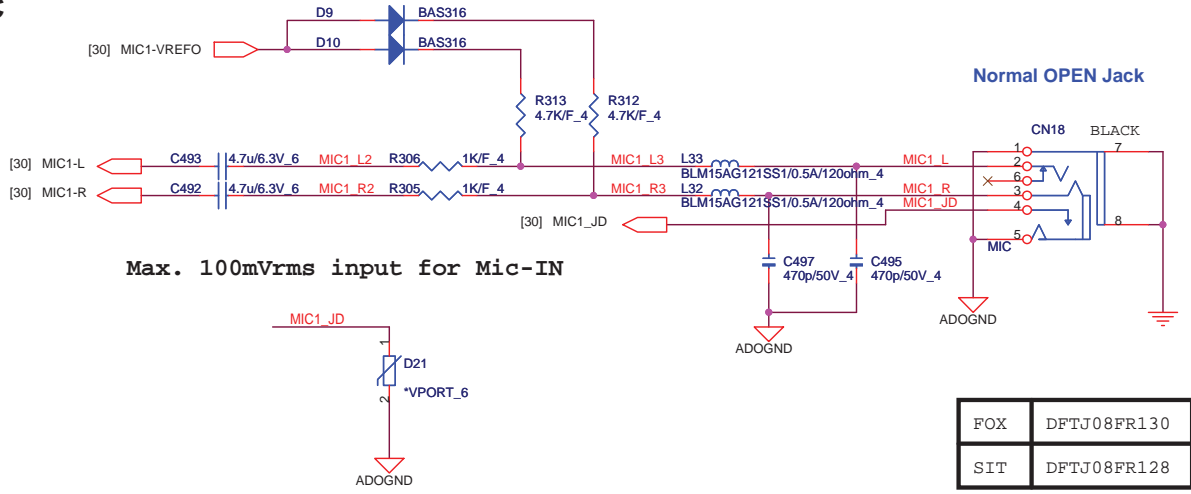
<http://hobi-elektronika.net/>

<http://hobi-elektronika.net/>

<http://hobi-elektronika.net/>

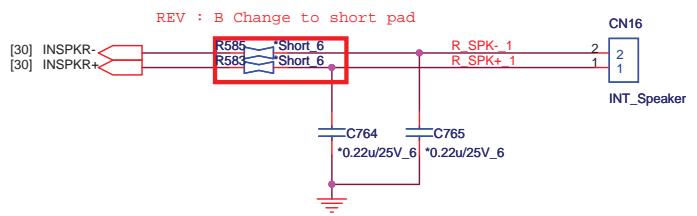
<http://hobi-elektronika.net/>





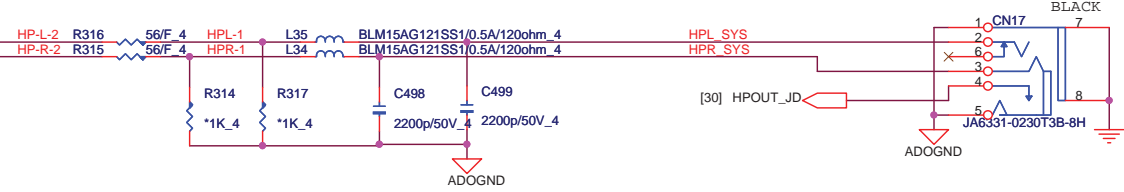
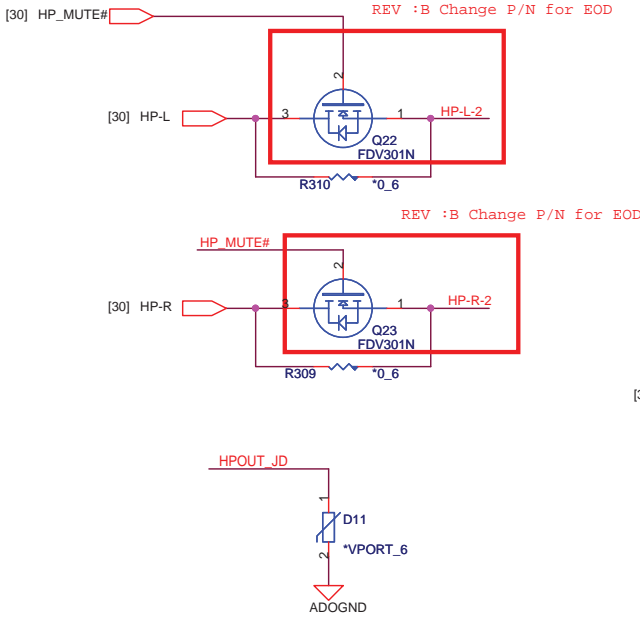
|     |             |
|-----|-------------|
| FOX | DFTJ08FR130 |
| SIT | DFTJ08FR128 |

Internal Speaker

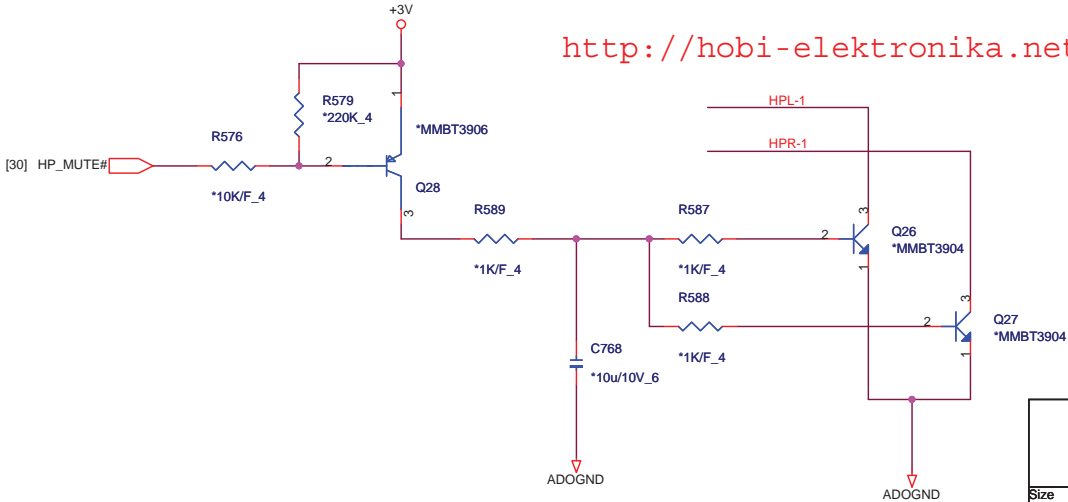


|     |             |
|-----|-------------|
| ACS | DFHD02MR311 |
| PTI | DFHD02MR508 |

HP/SPDIF



De-pop noise



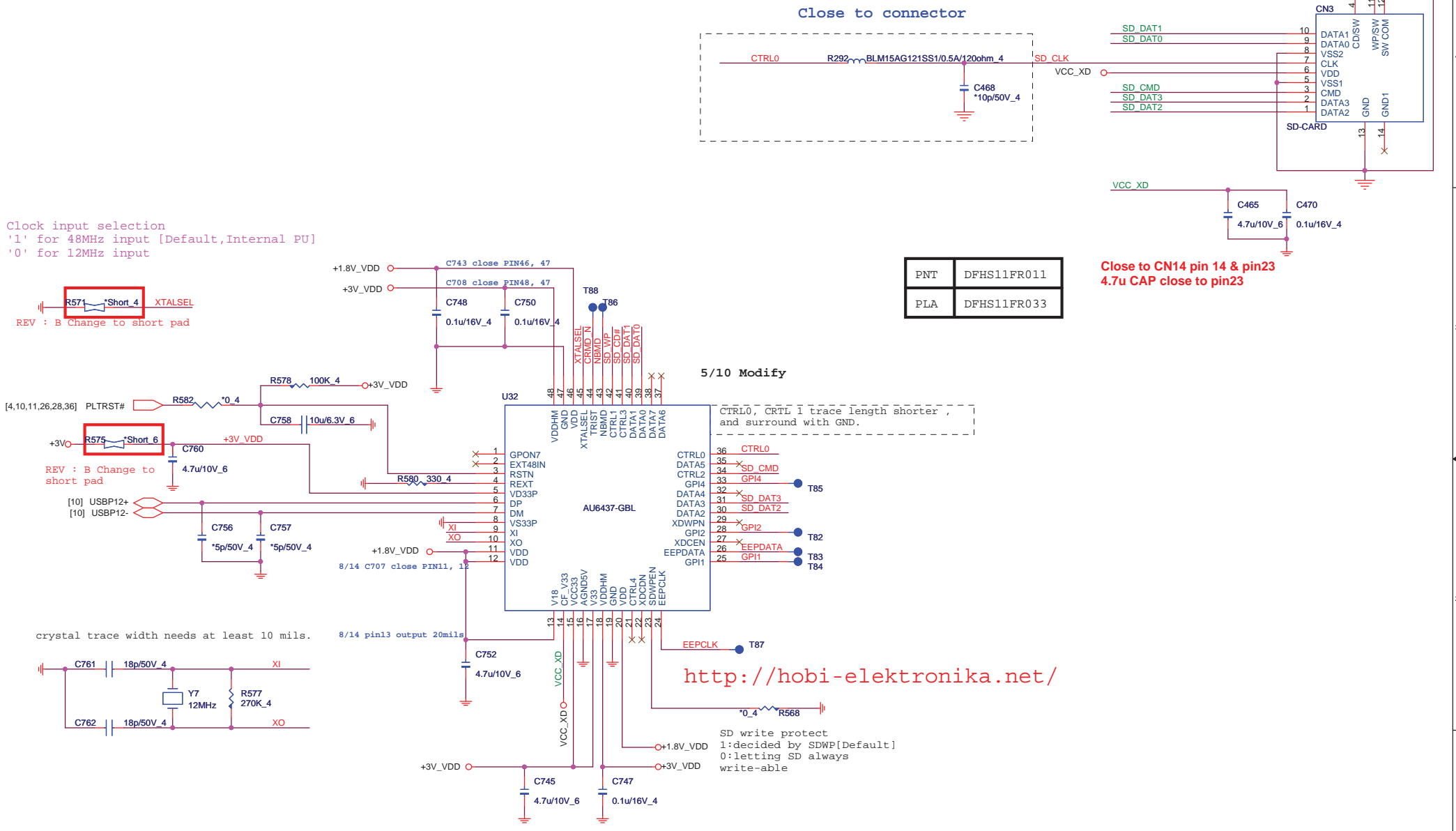
<http://hobi-elektronika.net/>

**Quanta Computer Inc.**  
PROJECT : ZRD

|       |                             |                |
|-------|-----------------------------|----------------|
| Size  | Document Number             | Rev            |
|       | <b>AMP /AUDIO JACK CONN</b> | 1C             |
| Date: | Wednesday, July 21, 2010    | Sheet 31 of 46 |

# CARD READER Controller

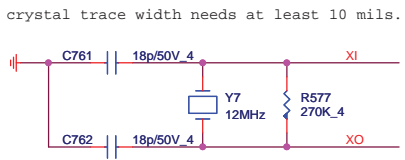
# 2 IN 1 CARD READER (SD/MMC)



Clock input selection  
 '1' for 48MHz input [Default, Internal PU]  
 '0' for 12MHz input

REV : B Change to short pad

REV : B Change to short pad



crystal trace width needs at least 10 mils.

|     |             |
|-----|-------------|
| PNT | DFHS11FR011 |
| PLA | DFHS11FR033 |

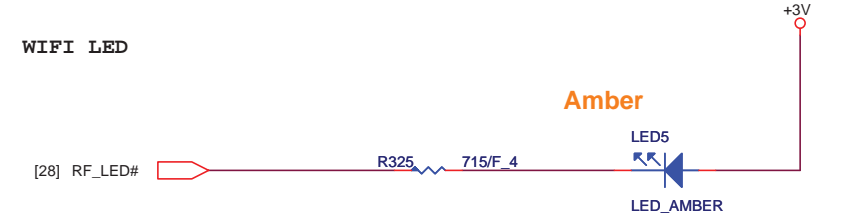
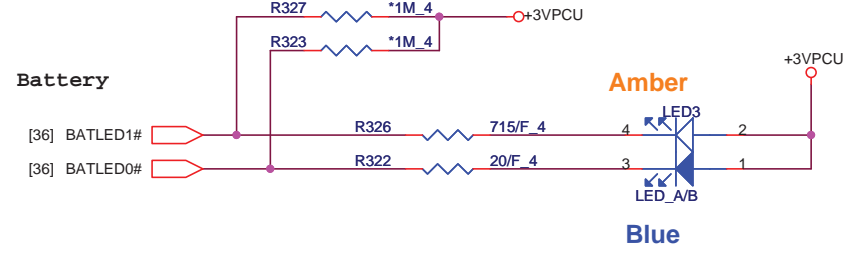
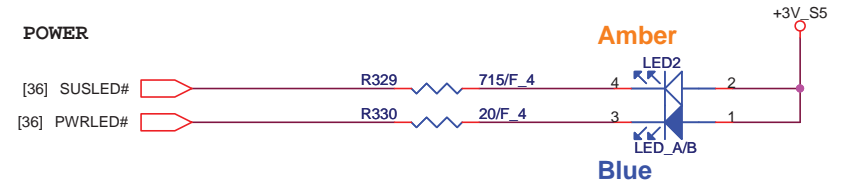
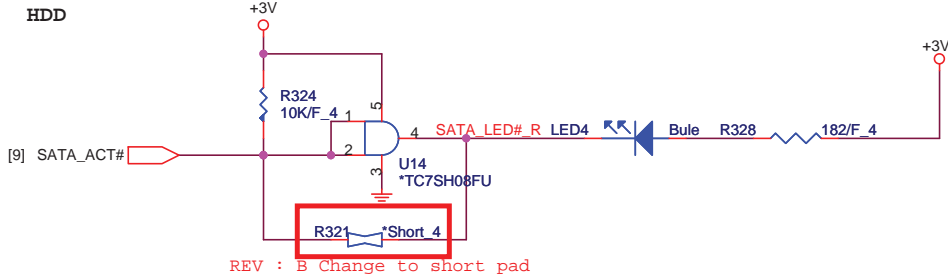
Close to CN14 pin 14 & pin23  
 4.7u CAP close to pin23


<http://hobi-elektronika.net/>

|                                       |  |   |
|---------------------------------------|--|---|
|                                       | <b>PROJECT : ZQ5</b><br>Quanta Computer Inc. |   |
|                                       | Size<br><b>AU6433 CardReader</b>             | Document Number<br><b>AU6433 CardReader</b> |
| Date: <b>Wednesday, July 21, 2010</b> |  | Sheet <b>32</b> of <b>43</b>                |

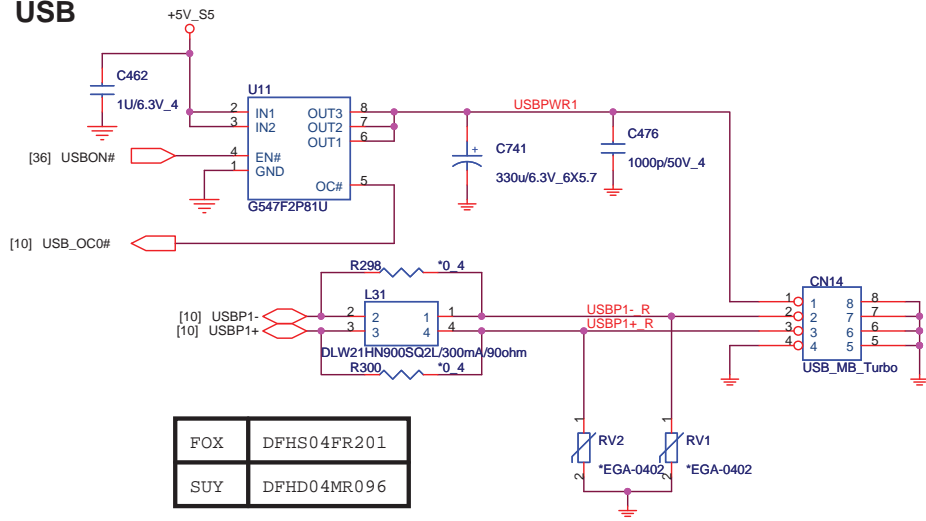


# LED



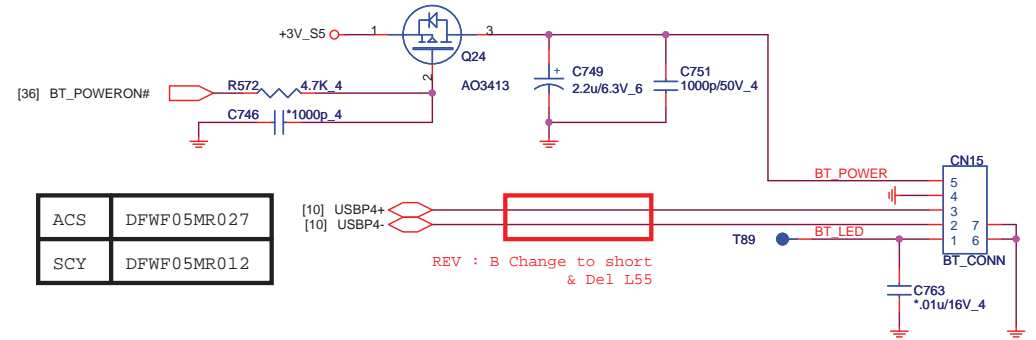
|  |  |       |                 |       |
|--|--|-------|-----------------|-------|
|  <b>Quanta Computer Inc.</b><br>PROJECT : ZRD |  | Size  | Document Number | Rev   |
|  |  |       |                 | 1C    |
| Date: Wednesday, July 21, 2010   |  | Sheet | 33              | of 46 |

# USB



|     |             |
|-----|-------------|
| FOX | DFHS04FR201 |
| SUY | DFHD04MR096 |

# BLUETOOTH CONNECTOR

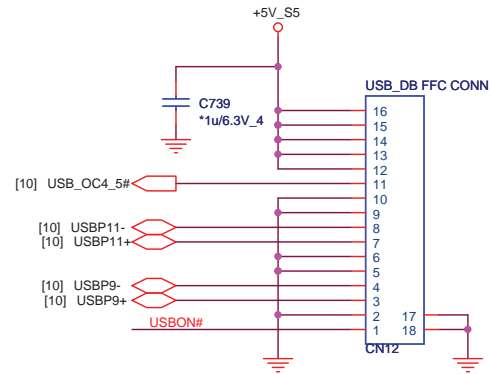



|     |             |
|-----|-------------|
| ACS | DFWF05MR027 |
| SCY | DFWF05MR012 |

REV : B Change to short & Del L55

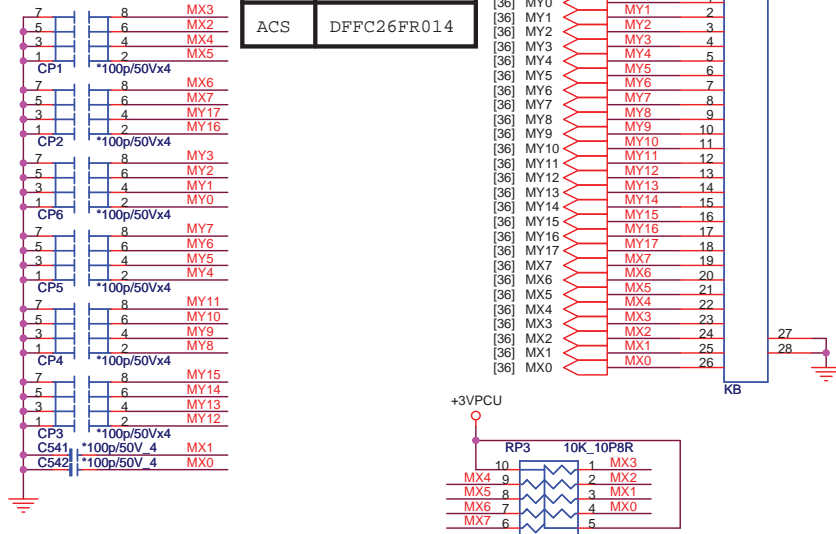
<http://hobi-elektronika.net/>

# USB/B



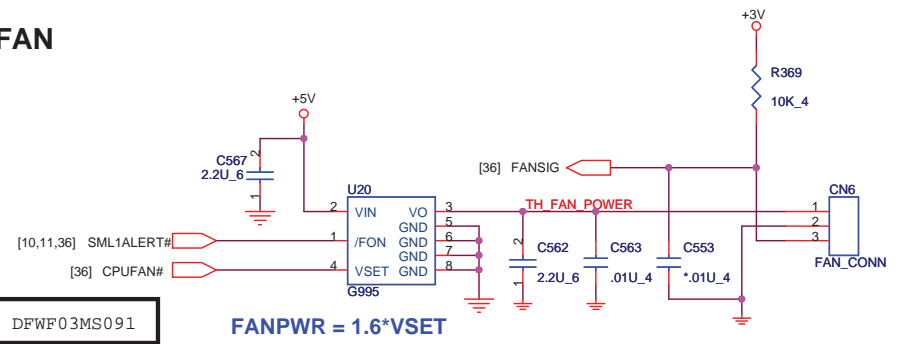
|   |  |       |                          |
|---|--|-------|--------------------------|
|  <b>Quanta Computer Inc.</b><br><b>PROJECT : ZRD</b> |  | Rev   | 1C                       |
|   |  | Size  | Document Number          |
| <b>USB/ BT</b>  |  | Date: | Wednesday, July 21, 2010 |
|   |  | Sheet | 34 of 46                 |

|     |             |
|-----|-------------|
| PTI | DFFC26FR155 |
| ACS | DFFC26FR014 |



### CPU FAN

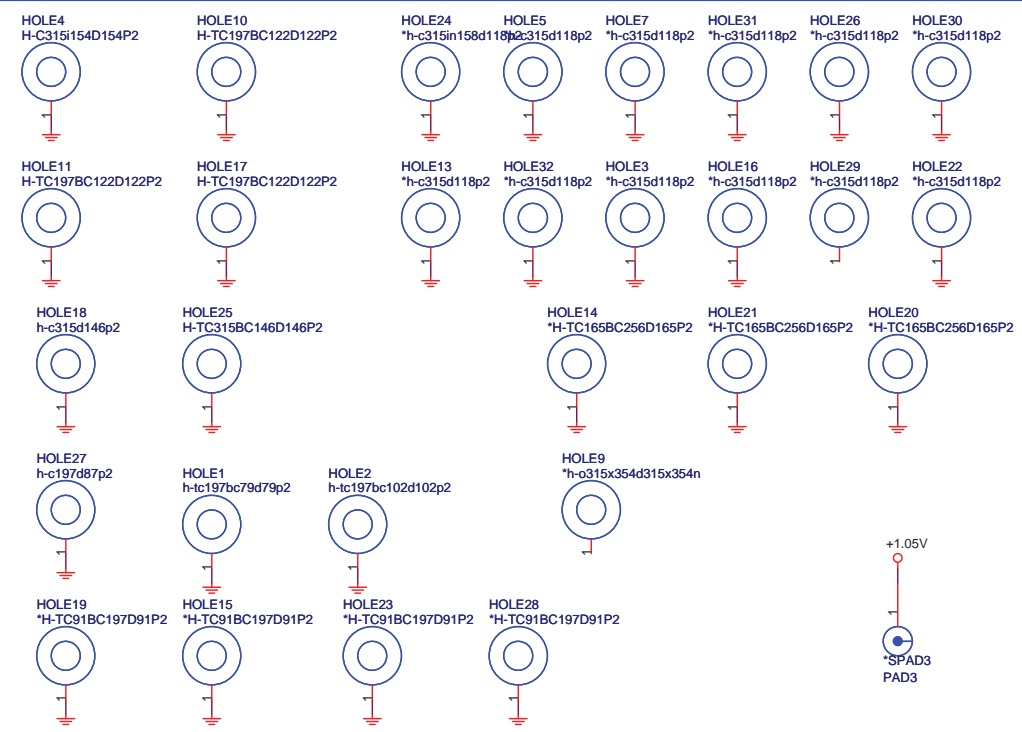
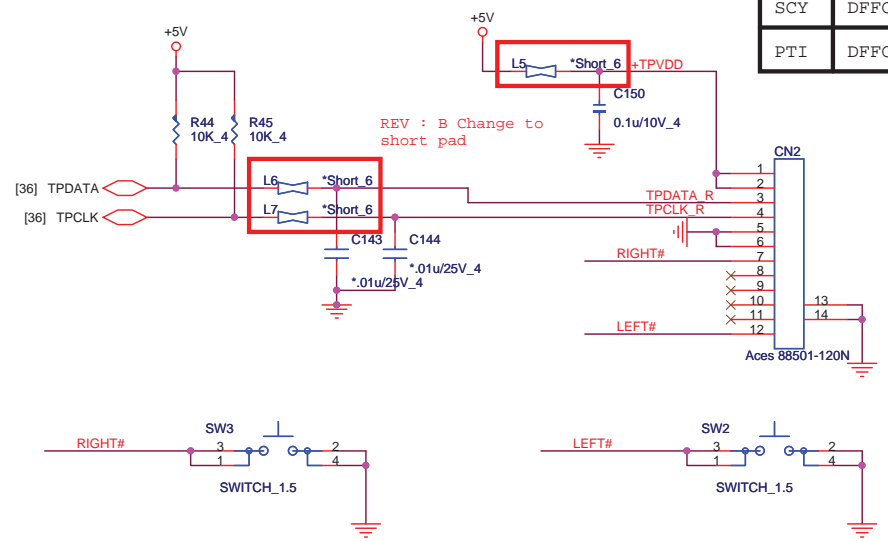
|     |             |
|-----|-------------|
| ACS | DFWF03MS091 |
| SCY | DFWF03MS000 |



FANPWR = 1.6 \* VSET

### TOUCHPAD & Switch CONN.

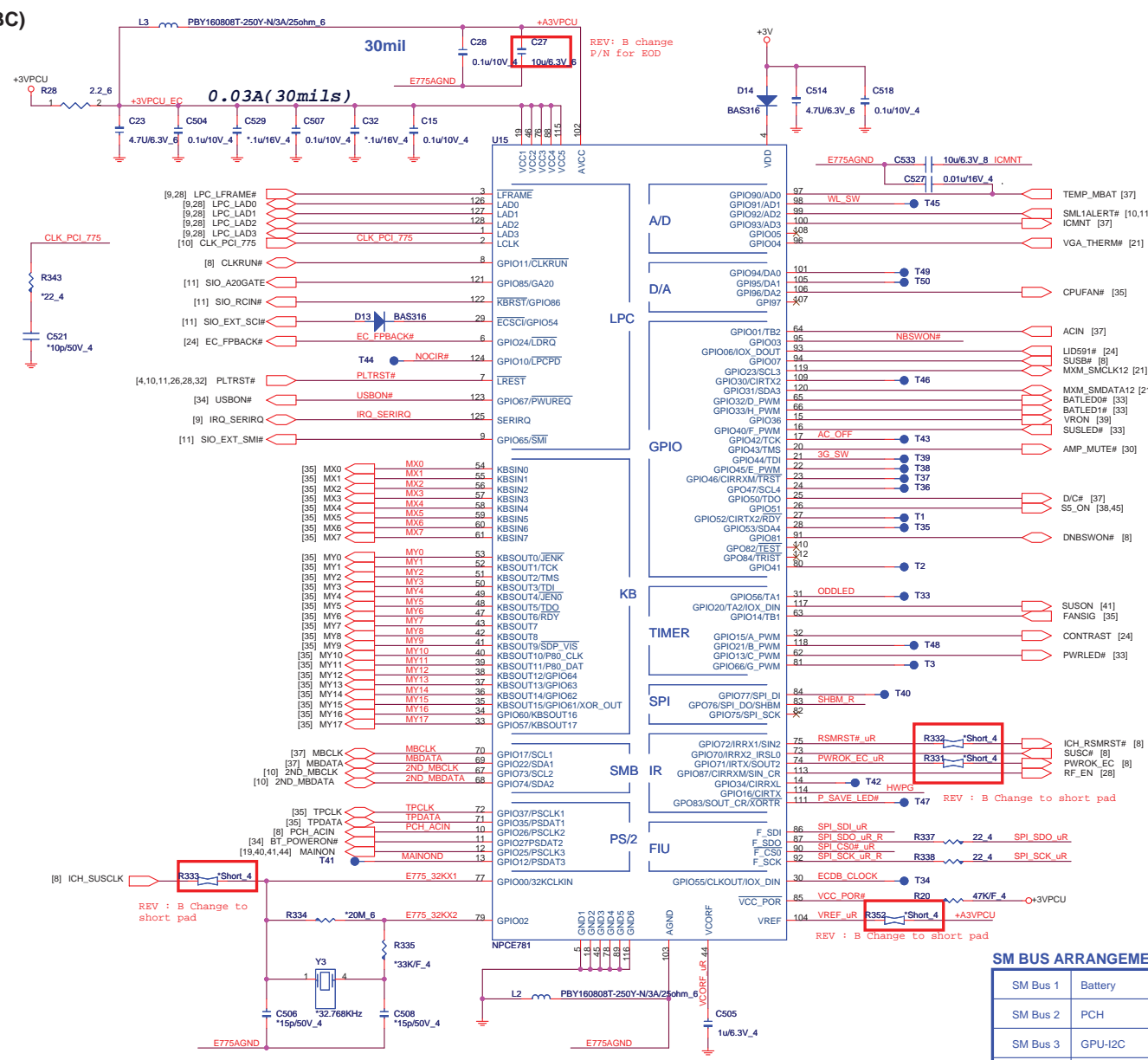
|     |             |
|-----|-------------|
| ACS | DFFC12FR017 |
| SCY | DFFC12FR015 |
| PTI | DFFC12FR234 |



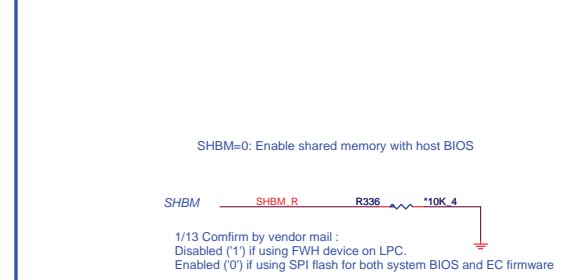
**Quanta Computer Inc.**  
**PROJECT : ZRD**

|      |                          |                |
|------|--------------------------|----------------|
| Size | Document Number          | Rev            |
|      | <b>KB/FAN/TP+FP</b>      | 1C             |
| Date | Wednesday, July 21, 2010 | Sheet 35 of 46 |

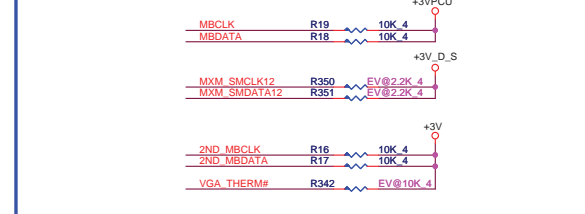
**EC(KBC)**



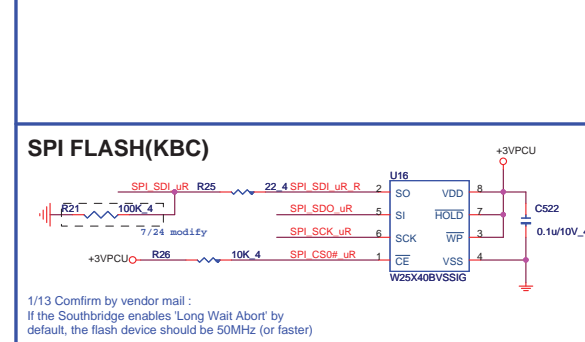
**I/O ADDRESS SETTING(KBC)**



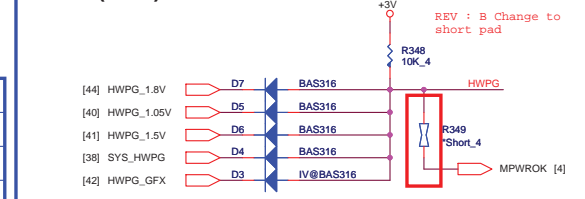
**SM BUS PU(KBC)**



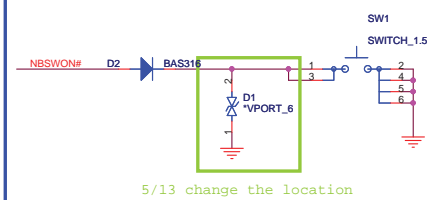
**SPI FLASH(KBC)**



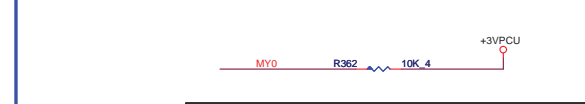
**HWPG(KBC)**



**POWER-ON Switch(KBC)**

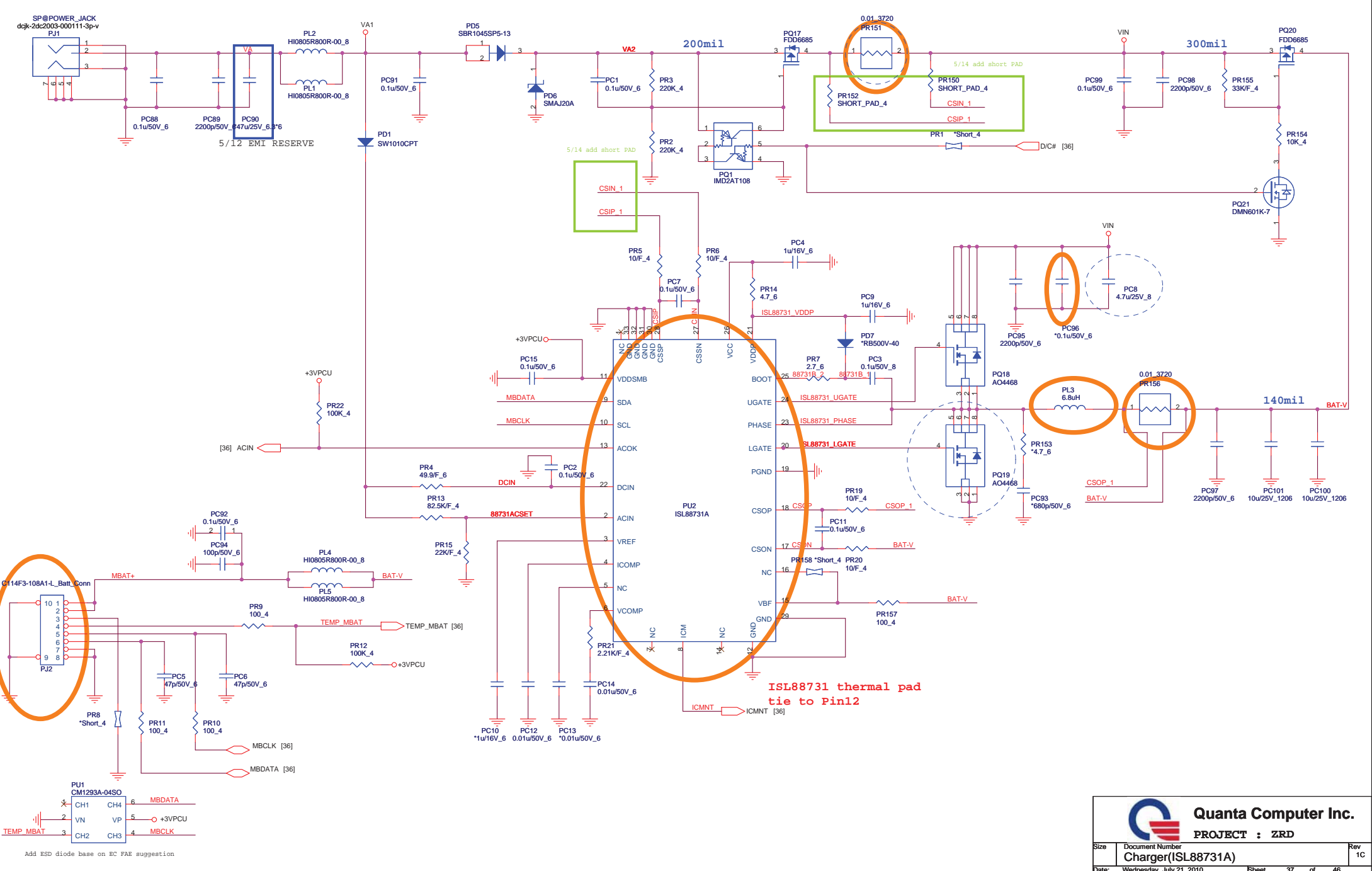


**INTERNAL KEYBOARD STRIP SET(KBC)**




**SM BUS ARRANGEMENT TABLE**

| SM Bus   | Device  |
|----------|---------|
| SM Bus 1 | Battery |
| SM Bus 2 | PCH     |
| SM Bus 3 | GPU-I2C |
| SM Bus 4 | N/A     |



ISL88731 thermal pad tie to Pin12

|  |                          |                |
|--|--------------------------|----------------|
|  <b>Quanta Computer Inc.</b><br>PROJECT : ZRD |                          | Rev            |
|  |                          | 1C             |
| Size   | Document Number          | Sheet 37 of 46 |
| Charger(ISL88731A)   |                          |                |
| Date:  | Wednesday, July 21, 2010 |                |

Add ESD diode base on EC FAE suggestion

200mil  
OCP: 6.5A  
5A

OCP: 6.5A  
 $L(\text{ripple current}) = (9-5) * 5 / (2.2u * 0.4M * 9) = 2.525A$   
 $I_{ocp} = 6.5 - (2.525 / 2) = 5.24A$   
 $V_{th} = 5.24A * 14.2m\Omega = 0.074V$   
 $R(I_{lim}) = (0.07437V * 10) / 5uA = 148.74K$   
 $I_{peak}(\text{choke}) = 10.687A$

OCP: 9A  
 $L(\text{ripple current}) = (9-3.3) * 3.3 / (2.2u * 0.5M * 9) = 1.9A$   
 $I_{ocp} = 9 - (1.9 / 2) = 8.05A$   
 $V_{th} = 8.05A * 14.2m\Omega = 114.31mV$   
 $R(I_{lim}) = (114.31mV * 10) / 5uA = 228.62K$   
 $I_{peak}(\text{choke}) = 11.479A$

2.85A  
114mil

2.171A  
87mil

3A  
107mil

10mil  
0.23A

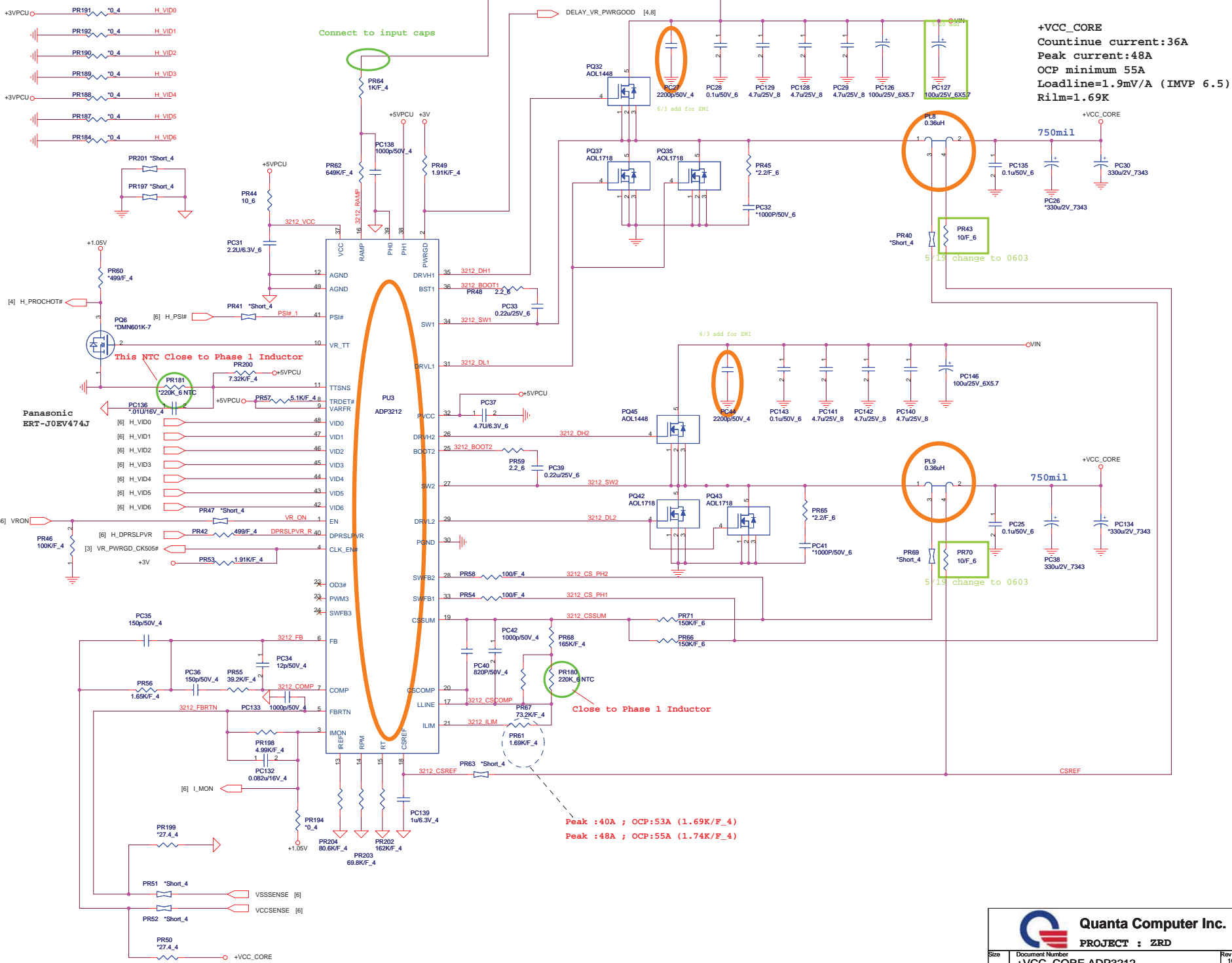
280mil  
OCP: 9A  
7A

**Quanta Computer Inc.**  
**PROJECT : ZRD**

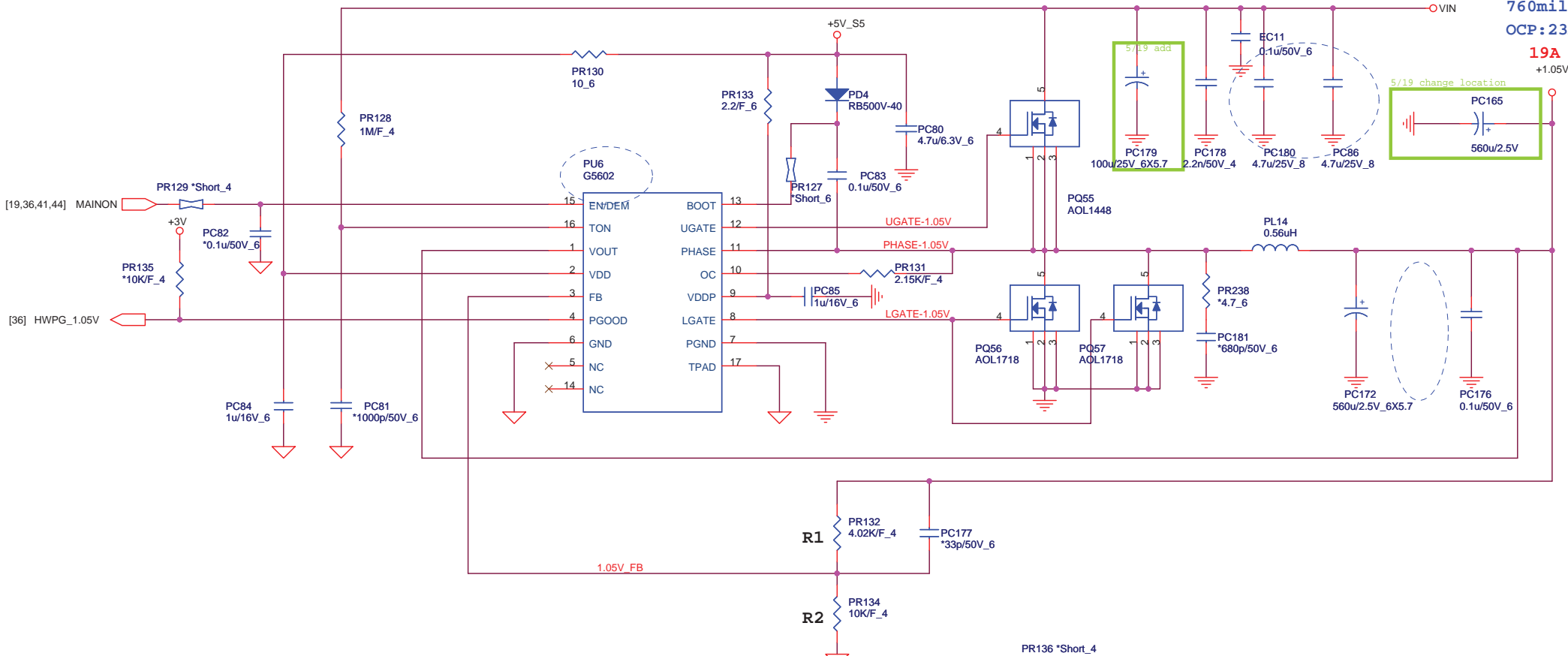
|      |                              |     |
|------|------------------------------|-----|
| Size | Document Number              | Rev |
|      | <b>SYSTEM 5V/3V (RT8206)</b> | 1C  |

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VID 1.2875V



[ PWM ]



760mil  
OCP: 23A  
19A  
+1.05V

$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$


$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

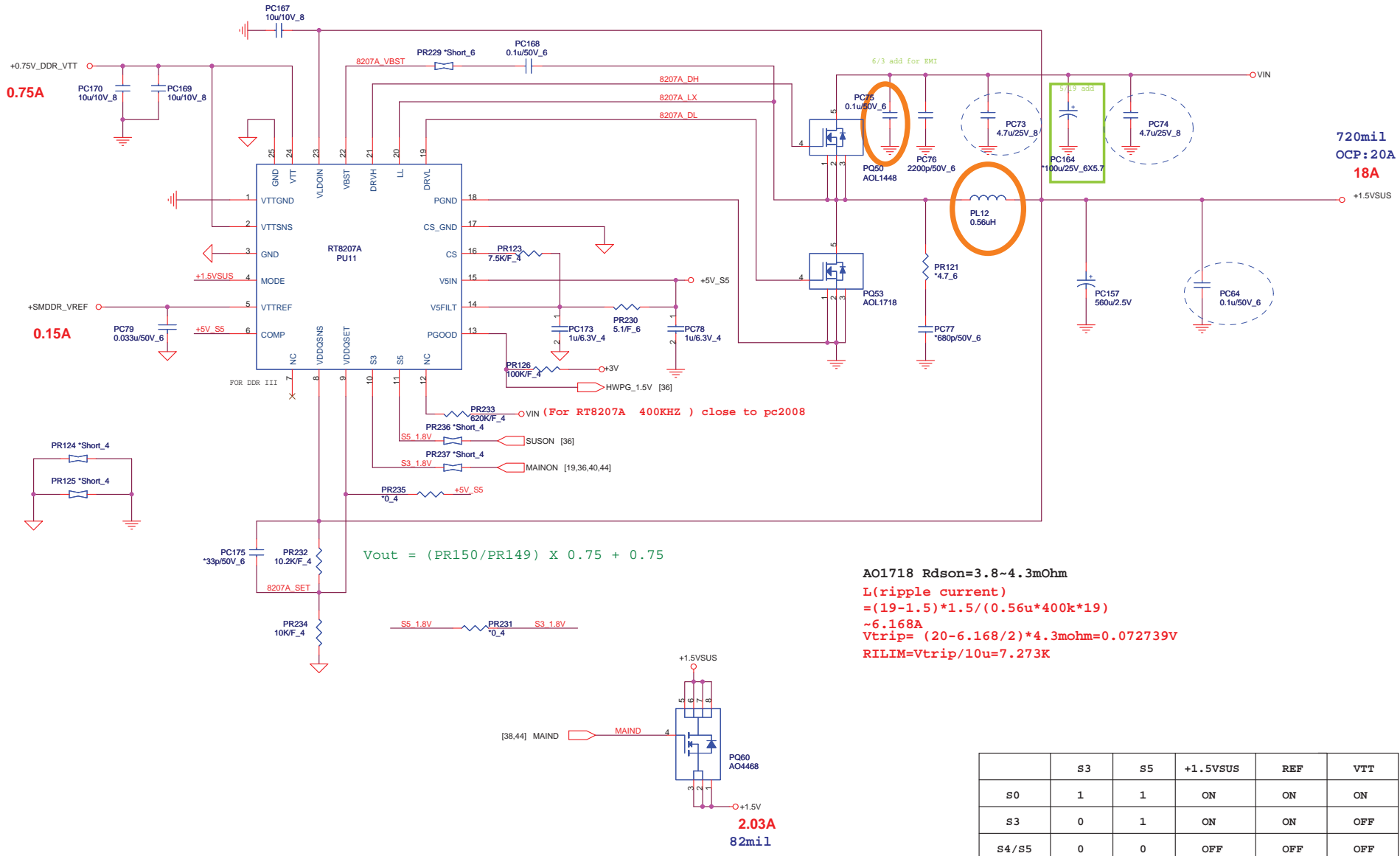
$$Frequency = 1 / (0.0036767) = 272K$$

AO1718  $R_{dson} = 3 \sim 4.3m\Omega$   
 $L(\text{ripple current}) = (19 - 1.05) * 1.05 / (0.56u * 272k * 19) \sim 6.512A$

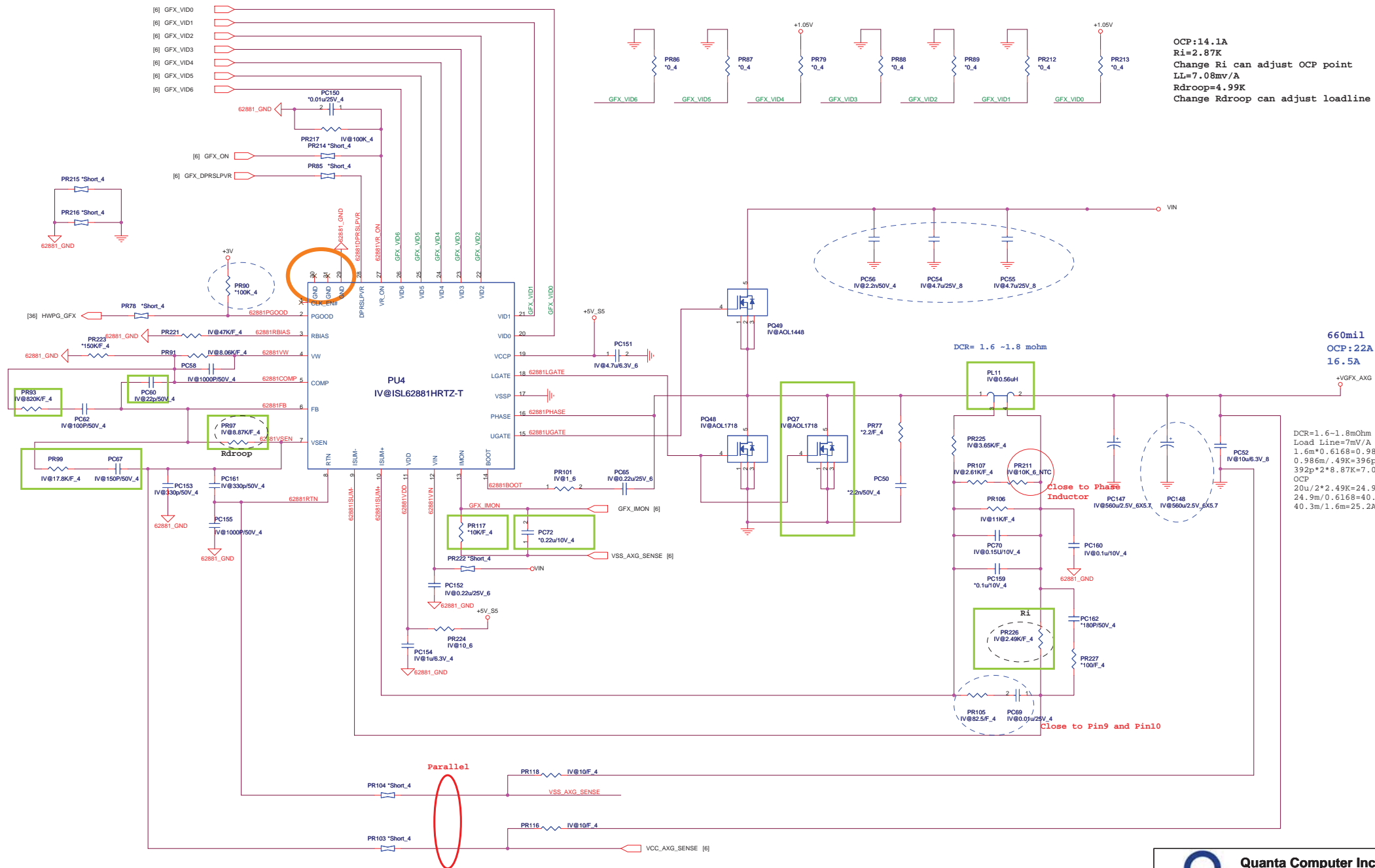
$RILIM = 2.15m\Omega * 23 - 3.256 / 20uA = 2.122K\Omega$   
 $I(\text{choke})_{peak} = 29.512A$

|  |                          |       |                       |     |
|--|--------------------------|-------|-----------------------|-----|
|  <b>Quanta Computer Inc.</b><br>PROJECT : ZRD |                          | Size  | Document Number       | Rev |
|  |                          |       | <b>+VTT (UP6111A)</b> | 1C  |
| Date:  | Wednesday, July 21, 2010 | Sheet | 40 of 46              |     |





|       | S3 | S5 | +1.5VSUS | REF | VTT |
|-------|----|----|----------|-----|-----|
| S0    | 1  | 1  | ON       | ON  | ON  |
| S3    | 0  | 1  | ON       | ON  | OFF |
| S4/S5 | 0  | 0  | OFF      | OFF | OFF |



OCP:14.1A  
 Ri=2.87K  
 Change Ri can adjust OCP point  
 LL=7.08mv/A  
 Rdroop=4.99K  
 Change Rdroop can adjust loadline

660mil  
 OCP:22A  
 16.5A

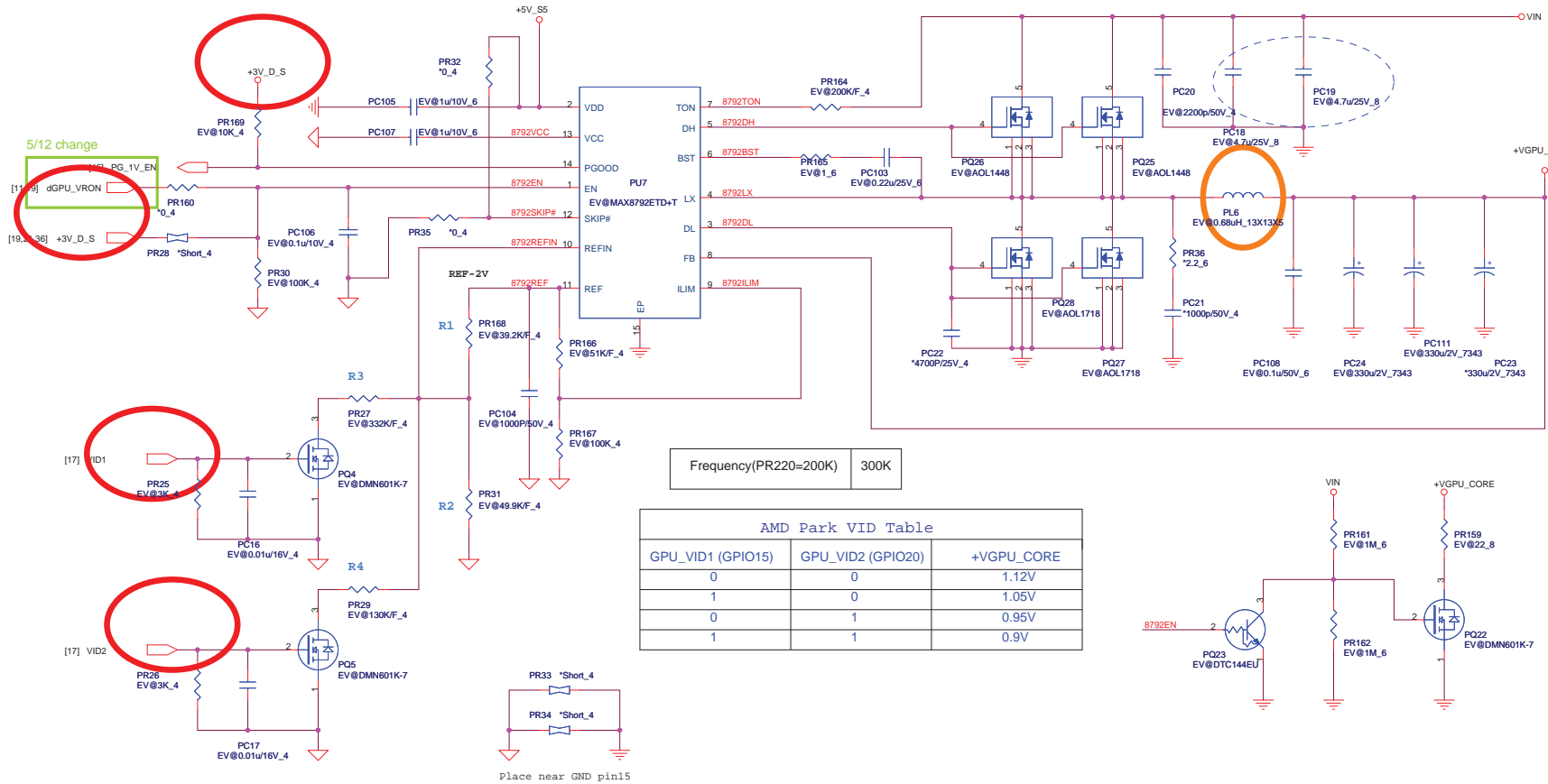
DCR=1.6~1.8mOhm  
 Load Line=7mV/A  
 1.6m\*0.6168=0.986m  
 0.986m/.49K=396p  
 392p\*2\*8.87K=7.03m  
 OCP  
 20u/2\*2.49K=24.9m  
 24.9m/0.6168=40.3m  
 40.3m/1.6m=25.2A

**Quanta Computer Inc.**  
 PROJECT : ZRD

|      |                      |     |
|------|----------------------|-----|
| Size | Document Number      | Rev |
|      | +VGF_X_AG (ISL62881) | 1C  |

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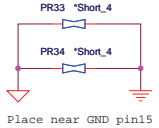
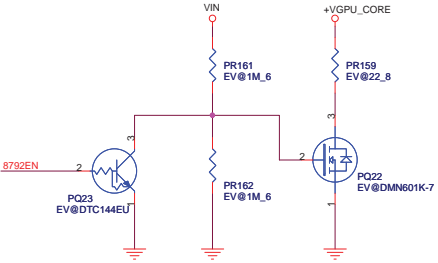
1. Level 1 Environment-related Substances should NEVER be used.  
 2. Purchase link, part, size, and holding status only from the business partners that only approves as green partners.



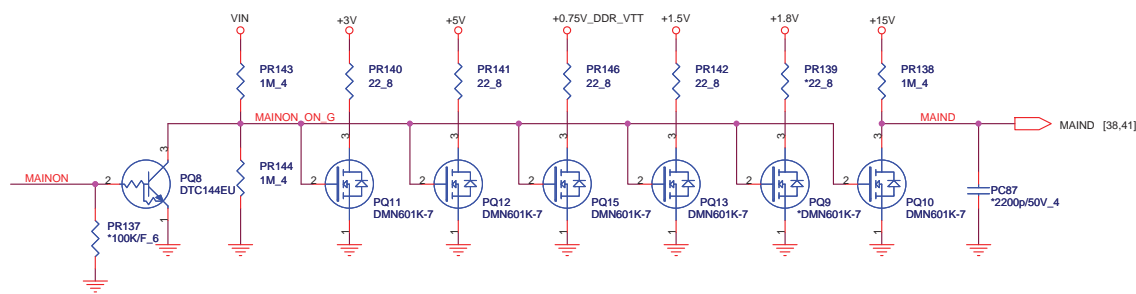
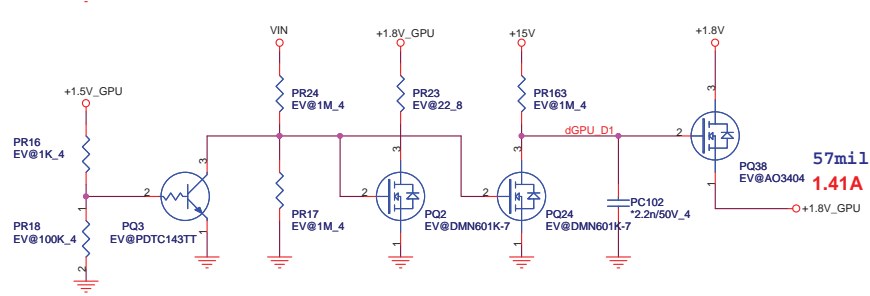
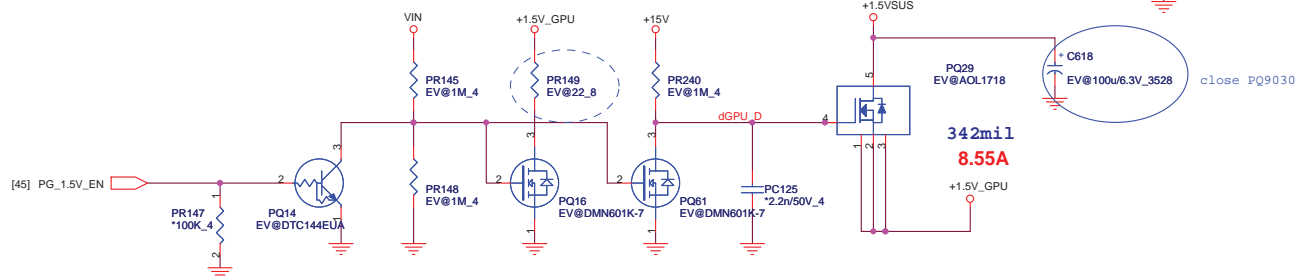
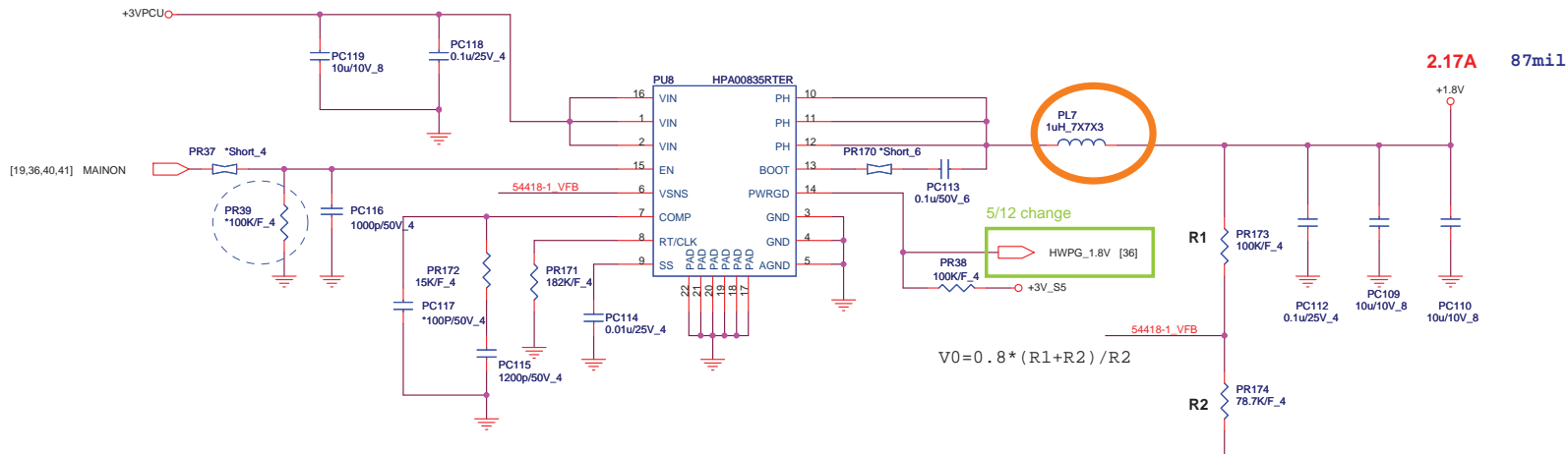
1050mil  
OCP=35A  
26.25A

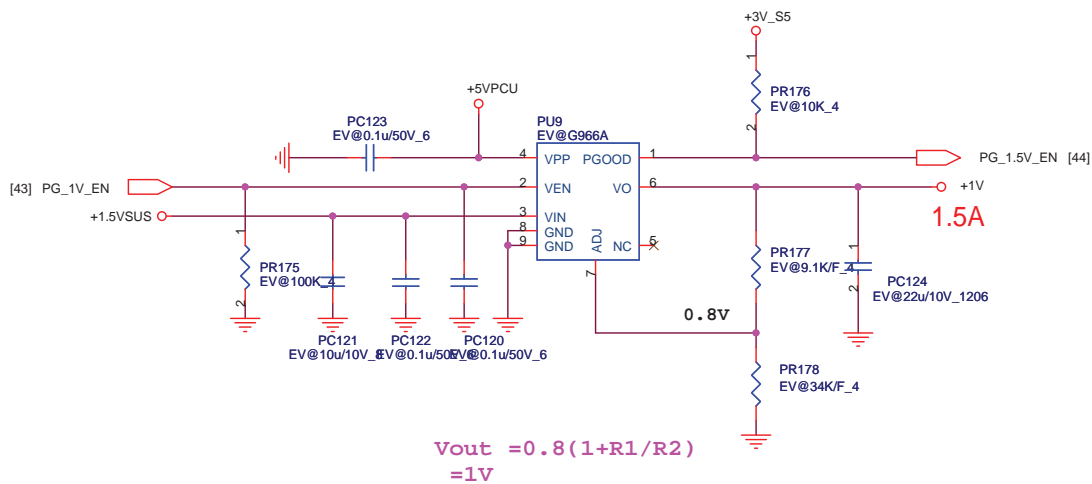
Frequency(PR220=200K) 300K

| GPU_VID1 (GPIO15) | GPU_VID2 (GPIO20) | +VGPU_CORE |
|-------------------|-------------------|------------|
| 0                 | 0                 | 1.12V      |
| 1                 | 0                 | 1.05V      |
| 0                 | 1                 | 0.95V      |
| 1                 | 1                 | 0.9V       |



**Quanta Computer Inc.**  
PROJECT : ZRD  
GPU CORE(MAX8792)  
Date: Wednesday, July 21, 2010 Sheet 43 of 9





**Thermal protection**

