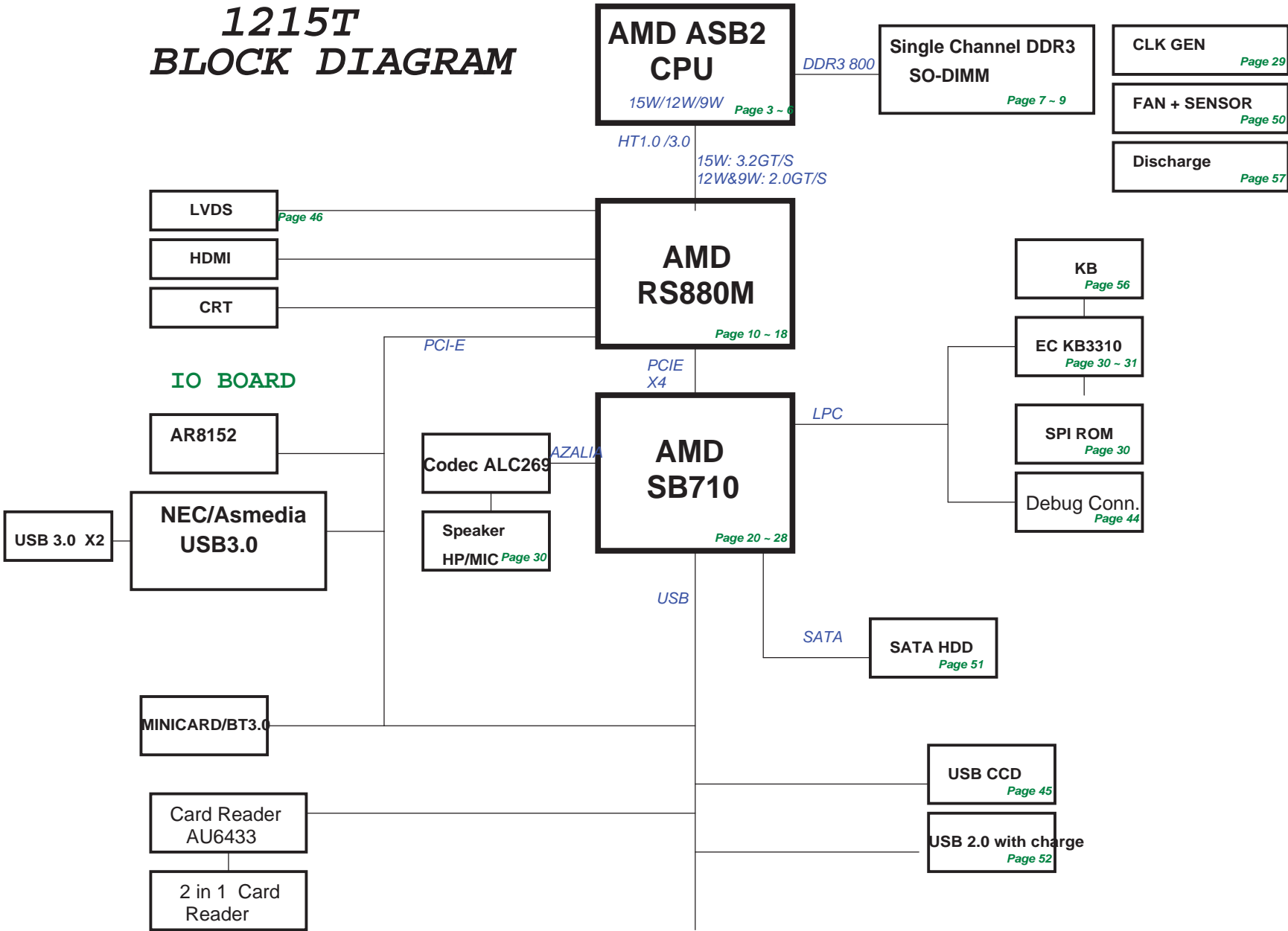
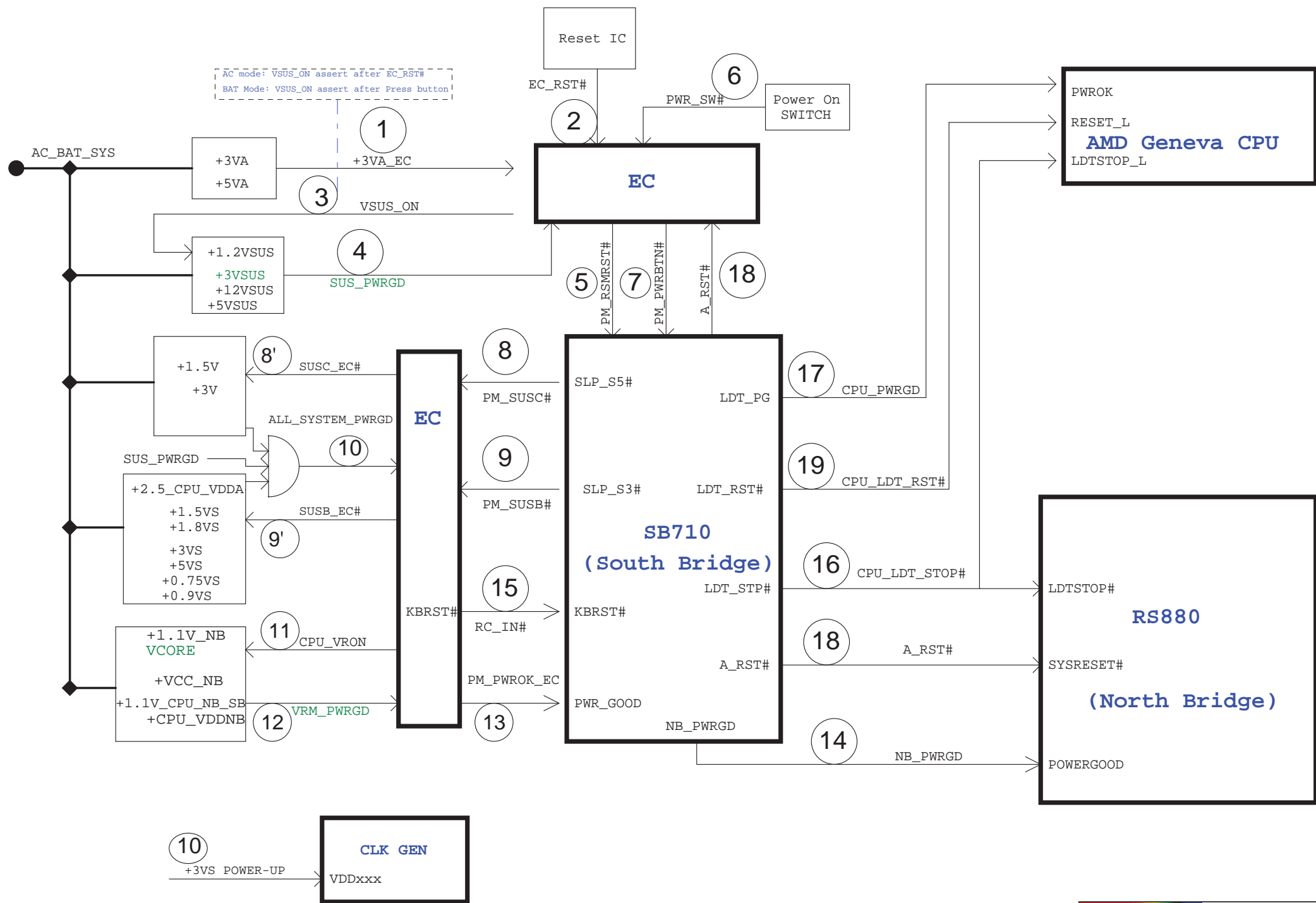


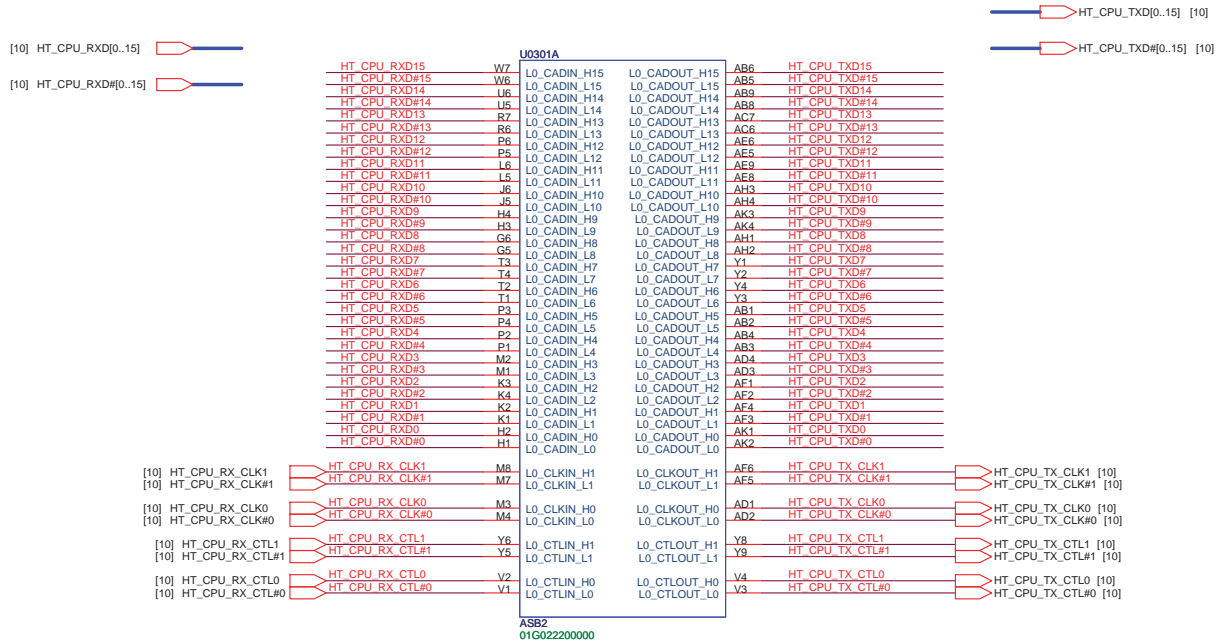
1215T BLOCK DIAGRAM



<Variant Name>

ASUS		Title : Block Diagram	
ASUSTeK Computer INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	1215T	1.0	
Date: Tuesday, August 10, 2010		Sheet	1 of 80





[7] H_D3A_MA[15..0]	H_D3A_MA15 P30	MA_ADD15
	H_D3A_MA14 M29	MA_ADD14
	H_D3A_MA13 AG28	MA_ADD13
	H_D3A_MA12 P28	MA_ADD12
	H_D3A_MA11 T30	MA_ADD11
	H_D3A_MA10 AC28	MA_ADD10
	H_D3A_MA9 R27	MA_ADD9
	H_D3A_MA8 R26	MA_ADD8
	H_D3A_MA7 R27	MA_ADD8
	H_D3A_MA6 Y20	MA_ADD7
	H_D3A_MA5 U28	MA_ADD6
	H_D3A_MA4 U27	MA_ADD5
	H_D3A_MA3 Y30	MA_ADD4
	H_D3A_MA2 AB29	MA_ADD3
	H_D3A_MA1 W29	MA_ADD2
	H_D3A_MA0 AC28	MA_ADD1
		MA_ADD0
	H_D3A_BA2 R29	MA_BANK2
	H_D3A_BA1 AC29	MA_BANK1
	H_D3A_BA0 AE28	MA_BANK0
		MA_BANK0
	-K30	MA_CHECK7
	-J29	MA_CHECK6
	-G29	MA_CHECK5
	-F29	MA_CHECK4
	-L28	MA_CHECK3
	-H29	MA_CHECK2
	-H29	MA_CHECK1
	-H27	MA_CHECK0
		MA_CHECK0
	-J27	MA_DQS_H8
	-J26	MA_DQS_L8
	H_D3A_DOSP7	MA_DQS_H7
	H_D3A_DOSP7	MA_DQS_L7
	H_D3A_DOSP6	MA_DQS_H6
	H_D3A_DOSP6	MA_DQS_L6
	H_D3A_DOSP5	MA_DQS_H5
	H_D3A_DOSP5	MA_DQS_L5
	H_D3A_DOSP4	MA_DQS_H4
	H_D3A_DOSP4	MA_DQS_L4
	H_D3A_DOSP3	MA_DQS_H3
	H_D3A_DOSP3	MA_DQS_L3
	H_D3A_DOSP2	MA_DQS_H2
	H_D3A_DOSP2	MA_DQS_L2
	H_D3A_DOSP1	MA_DQS_H1
	H_D3A_DOSP1	MA_DQS_L1
	H_D3A_DOSP0	MA_DQS_H0
	H_D3A_DOSP0	MA_DQS_L0
		MA_DQS_L0
	AK18	MA_CLK_H7
	AJ17	MA_CLK_L7
	AH17	MA_CLK_H6
	AG17	MA_CLK_L6
	Y28	MA_CLK_H5
	Y27	MA_CLK_L5
	AB27	MA_CLK_H4
	AB26	MA_CLK_L4
	-W27	MA_CLK_H3
	-W26	MA_CLK_L3
	-P26	MA_CLK_H2
	-M26	MA_CLK_L2
	-D18	MA_CLK_H1
	-E19	MA_CLK_L1
	-E20	MA_CLK_H0
	-E19	MA_CLK_L0
		MA_CLK_L0
[7] H_D3A_CKE1	M30	MA_CKE1
[7] H_D3A_CKE0	M29	MA_CKE0
	AJ29	RSVD7
	AE27	RSVD7
	AJ30	RSVD7
[7] H_D3A_ODT1	AG29	MA0_ODT1
[7] H_D3A_ODT0	AG29	MA0_ODT0
	AH29	RSVD4
	AE29	RSVD1
	AH30	MA0_CS_L1
	AE29	MA0_CS_L0
[7] H_D3A_RAS#	AC27	MA_RAS_L
[7] H_D3A_CAS#	AE30	MA_CAS_L
[7] H_D3A_WE#	AE27	MA_WE_L
		MA_WE_L
[7] H_D3A_DRAMRST#	L27	MA_RESET_L
[7] H_PM_EXT_TSM0	M32	MA_EVENT_L

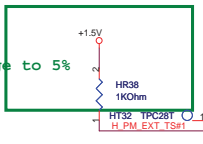
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MA_DATA62	AH11	H_D3A_DQ62	
MA_DATA61	AJ12	H_D3A_DQ61	
MA_DATA60	AJ14	H_D3A_DQ60	
MA_DATA59	AE11	H_D3A_DQ59	
MA_DATA58	AE12	H_D3A_DQ58	
MA_DATA57	AG12	H_D3A_DQ57	
MA_DATA56	AH12	H_D3A_DQ56	
MA_DATA55	AK14	H_D3A_DQ55	
MA_DATA54	AE15	H_D3A_DQ54	
MA_DATA53	AH10	H_D3A_DQ53	
MA_DATA52	AK20	H_D3A_DQ52	
MA_DATA51	AE14	H_D3A_DQ51	
MA_DATA50	AG14	H_D3A_DQ50	
MA_DATA49	AE17	H_D3A_DQ49	
MA_DATA48	AG10	H_D3A_DQ48	
MA_DATA47	AG20	H_D3A_DQ47	
MA_DATA46	AJ20	H_D3A_DQ46	
MA_DATA45	AE22	H_D3A_DQ45	
MA_DATA44	AK24	H_D3A_DQ44	
MA_DATA43	AE20	H_D3A_DQ43	
MA_DATA42	AJ23	H_D3A_DQ42	
MA_DATA41	AE23	H_D3A_DQ41	
MA_DATA40	AG23	H_D3A_DQ40	
MA_DATA39	AE25	H_D3A_DQ39	
MA_DATA38	AE25	H_D3A_DQ38	
MA_DATA37	AH27	H_D3A_DQ37	
MA_DATA36	AK30	H_D3A_DQ36	
MA_DATA35	AJ25	H_D3A_DQ35	
MA_DATA34	AG25	H_D3A_DQ34	
MA_DATA33	AJ28	H_D3A_DQ33	
MA_DATA32	AJ28	H_D3A_DQ32	
MA_DATA31	G28	H_D3A_DQ31	
MA_DATA30	D26	H_D3A_DQ30	
MA_DATA29	E26	H_D3A_DQ29	
MA_DATA28	F20	H_D3A_DQ27	
MA_DATA27	E20	H_D3A_DQ26	
MA_DATA26	F27	H_D3A_DQ25	
MA_DATA25	H26	H_D3A_DQ24	
MA_DATA24	D24	H_D3A_DQ23	
MA_DATA23	H22	H_D3A_DQ21	
MA_DATA22	E22	H_D3A_DQ20	
MA_DATA21	F26	H_D3A_DQ19	
MA_DATA20	G26	H_D3A_DQ18	
MA_DATA19	D22	H_D3A_DQ17	
MA_DATA18	G23	H_D3A_DQ16	
MA_DATA17	G22	H_D3A_DQ15	
MA_DATA16	G20	H_D3A_DQ14	
MA_DATA15	G15	H_D3A_DQ13	
MA_DATA14	F15	H_D3A_DQ12	
MA_DATA13	D20	H_D3A_DQ11	
MA_DATA12	F22	H_D3A_DQ10	
MA_DATA11	D16	H_D3A_DQ9	
MA_DATA10	E17	H_D3A_DQ8	
MA_DATA9	H15	H_D3A_DQ7	
MA_DATA8	H14	H_D3A_DQ6	
MA_DATA7	G12	H_D3A_DQ5	
MA_DATA6	H12	H_D3A_DQ4	
MA_DATA5	E15	H_D3A_DQ3	
MA_DATA4	E14	H_D3A_DQ2	
MA_DATA3	E11	H_D3A_DQ1	
MA_DATA2	F11	H_D3A_DQ0	
MA_DATA1			
MA_DATA0			
	H30	H_D3A_DM7	
	AK16	H_D3A_DM6	
	AK22	H_D3A_DM5	
	MA_DM5	AJ27	H_D3A_DM4
	MA_DM4	E27	H_D3A_DM3
	MA_DM3	E23	H_D3A_DM2
	MA_DM2	H19	H_D3A_DM1
	MA_DM1	G14	H_D3A_DM0
	MA_DM0		

<< >> H_D3A_DQ[63..0] [7]
 >> H_D3A_BA[2..0] [7]
 << >> H_D3A_DQSP[7..0] [7]
 << >> H_D3A_DQSN[7..0] [7]

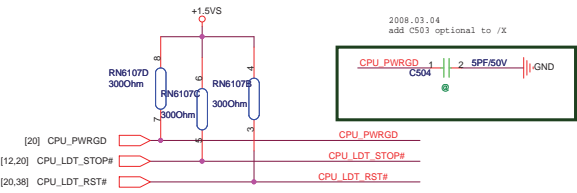
<< >> H_D3A_DM[7..0] [7]

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-P31	MB_ADD14	MB_DATA62	AL14
AK33	MB_ADD13	MB_DATA61	AL16
-I32	MB_ADD12	MB_DATA60	AN17
-I31	MB_ADD11	MB_DATA59	AN12
AD32	MB_ADD10	MB_DATA58	AM12
-I33	MB_ADD9	MB_DATA57	AM16
-I32	MB_ADD8	MB_DATA56	AN18
UK33	MB_ADD7	MB_DATA55	AL18
-U33	MB_ADD6	MB_DATA54	AN19
-V31	MB_ADD5	MB_DATA53	AM24
AK33	MB_ADD4	MB_DATA52	AN24
-V31	MB_ADD3	MB_DATA51	AM18
AK33	MB_ADD2	MB_DATA50	AN18
AK33	MB_ADD1	MB_DATA49	AL22
AK33	MB_ADD0	MB_DATA48	AN23
		MB_DATA47	AM26
R33	MB_BANK2	MB_DATA46	AL26
AD33	MB_BANK1	MB_DATA45	AN28
AE33	MB_BANK0	MB_DATA44	AL24
		MB_DATA43	AN25
-K33	MB_CHECK7	MB_DATA42	AN27
-K31	MB_CHECK6	MB_DATA41	AM28
-G32	MB_CHECK5	MB_DATA40	AM29
-F32	MB_CHECK4	MB_DATA39	AM29
L33	MB_CHECK3	MB_DATA38	AL32
K32	MB_CHECK2	MB_DATA37	AL33
H41	MB_CHECK1	MB_DATA36	AK28
-G33	MB_CHECK0	MB_DATA35	AN29
		MB_DATA34	AM31
-J33	MB_DQS_H8	MB_DATA33	AM32
-I32	MB_DQS_L8	MB_DATA32	E33
AM14	MB_DQS_H7	MB_DATA31	D31
AM14	MB_DQS_L7	MB_DATA30	E31
AL20	MB_DQS_H6	MB_DATA29	A31
AM20	MB_DQS_H5	MB_DATA28	F31
AK26	MB_DQS_L5	MB_DATA27	F31
AM26	MB_DQS_H4	MB_DATA26	C32
AK30	MB_DQS_L4	MB_DATA25	C30
AK30	MB_DQS_H3	MB_DATA24	C30
-D32	MB_DQS_L3	MB_DATA23	A29
B28	MB_DQS_H2	MB_DATA22	B28
A28	MB_DQS_L2	MB_DATA21	A26
A21	MB_DQS_H1	MB_DATA20	B30
B20	MB_DQS_L1	MB_DATA19	A30
B16	MB_DQS_H0	MB_DATA18	A27
A15	MB_DQS_L0	MB_DATA17	C26
		MB_DATA16	A24
AN22	MB_CLK_H7	MB_DATA15	B24
AM22	MB_CLK_L7	MB_DATA14	C18
AM21	MB_CLK_H6	MB_DATA13	A18
AM21	MB_CLK_L6	MB_DATA12	A25
AA32	MB_CLK_H5	MB_DATA11	C24
AB33	MB_CLK_L5	MB_DATA10	C20
AB33	MB_CLK_H4	MB_DATA9	A19
AB32	MB_CLK_L4	MB_DATA8	C18
AB31	MB_CLK_H3	MB_DATA7	A16
AB30	MB_CLK_L3	MB_DATA6	B14
AD31	MB_CLK_H2	MB_DATA5	A13
AD30	MB_CLK_L2	MB_DATA4	A18
C22	MB_CLK_H1	MB_DATA3	A17
E22	MB_CLK_L1	MB_DATA2	C14
A22	MB_CLK_H0	MB_DATA1	A14
A23	MB_CLK_L0	MB_DATA0	A14
		MB_DM8	H33
N33	MB_CKE1	MB_DM7	AN15
P32	MB_CKE0	MB_DM6	AN20
		MB_DM5	AK26
		MB_DM4	AN31
AK31	RSVD9	MB_DM3	C33
AH31	RSVD5	MB_DM2	C28
AK32	MB0_ODT1	MB_DM1	A20
AH33	MB0_ODT0	MB_DM0	D14
AK33	RSVD10		
AE33	MB0_CS_L1		
AE31	MB0_CS_L0		
		MB_RAS_L	
AE32	MB_CAS_L		
AG33	MB_WE_L		
		MB_RESET_L	
L32	MB_EVENT_L		
M33			

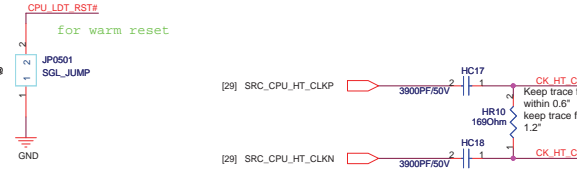
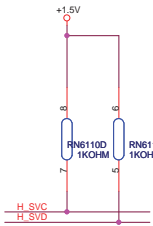
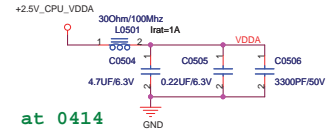
R1.1
1% change to 5%



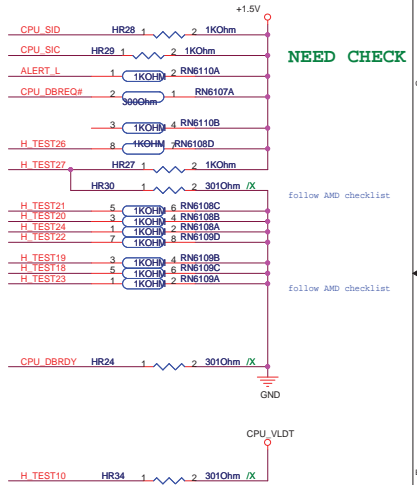
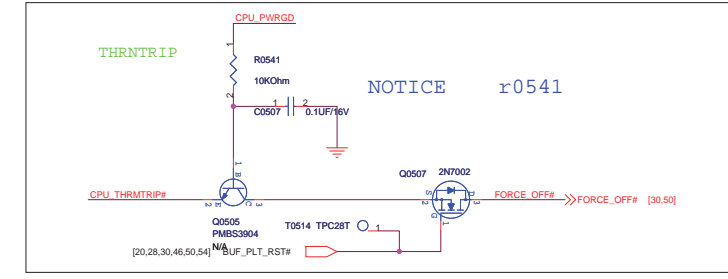
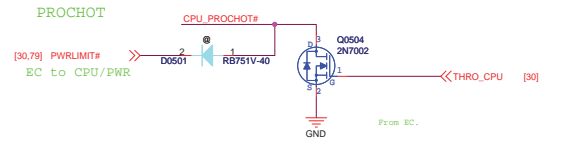
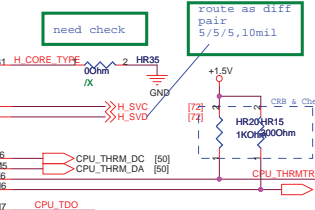
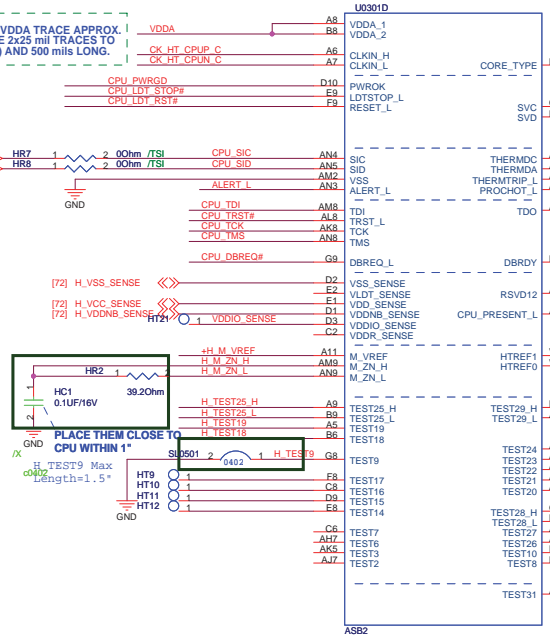
Change list:
1. CLK 0 and 1 reserved follow AMD Schematic check list.



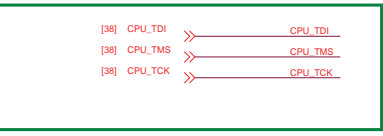
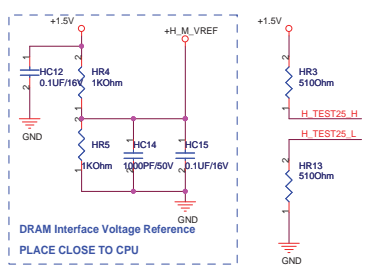
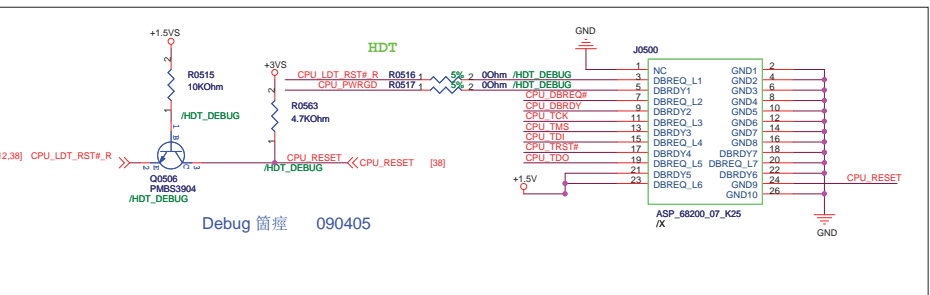
DEL C0503 at 0414



LAYOUT: ROUTE VDDA TRACE APPROX. 1 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.



NEED CHECK



ACC

ASUS Logo

ASUSTeK Computer, INC. Title: Gonesus CNT/DBG/THE BM
Engineer: N/A

Size	Project Name	Rev
C	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 5 of 80

DESIGN NOTE:
 VLDT must be routed as a pour or a trace at least 200 mils wide.
 VLDT may be routed from the source to either ALx balls or Fx balls.
 Choose whichever makes routing simpler.
 These six capacitors must be placed very near the selected balls.
 The other set of balls must be decoupled with a 4.7uF cap.

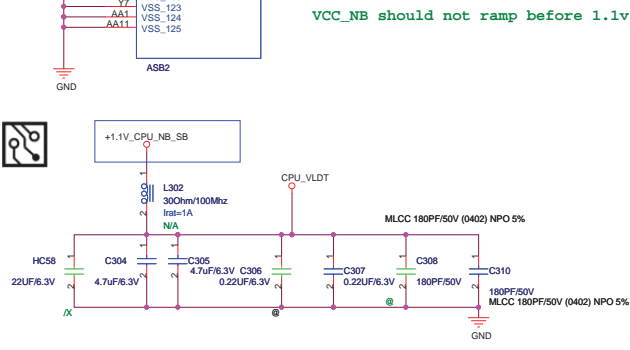
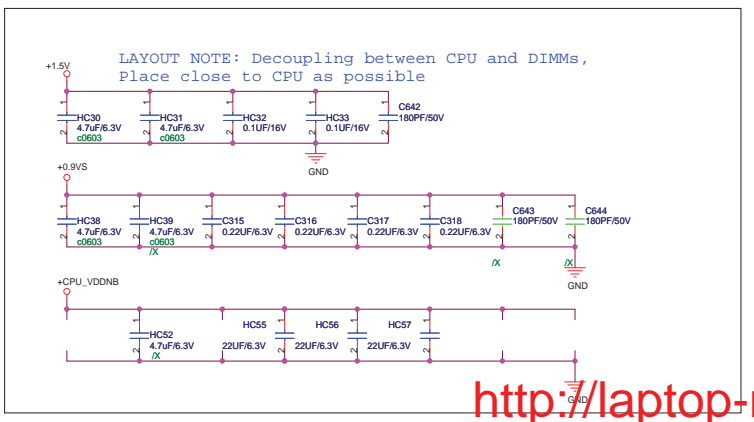
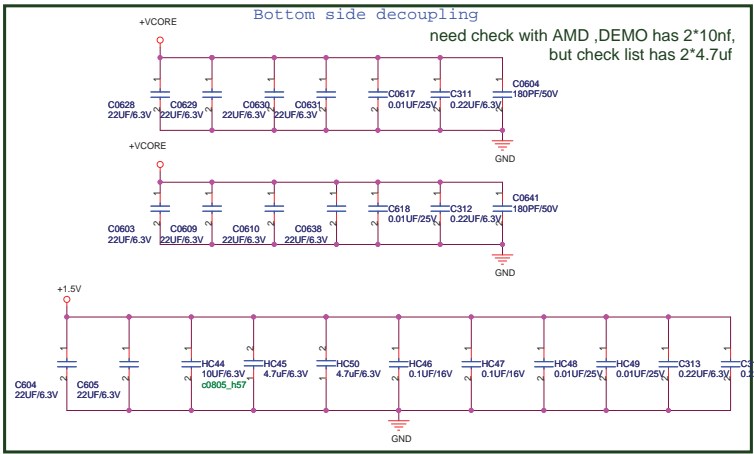
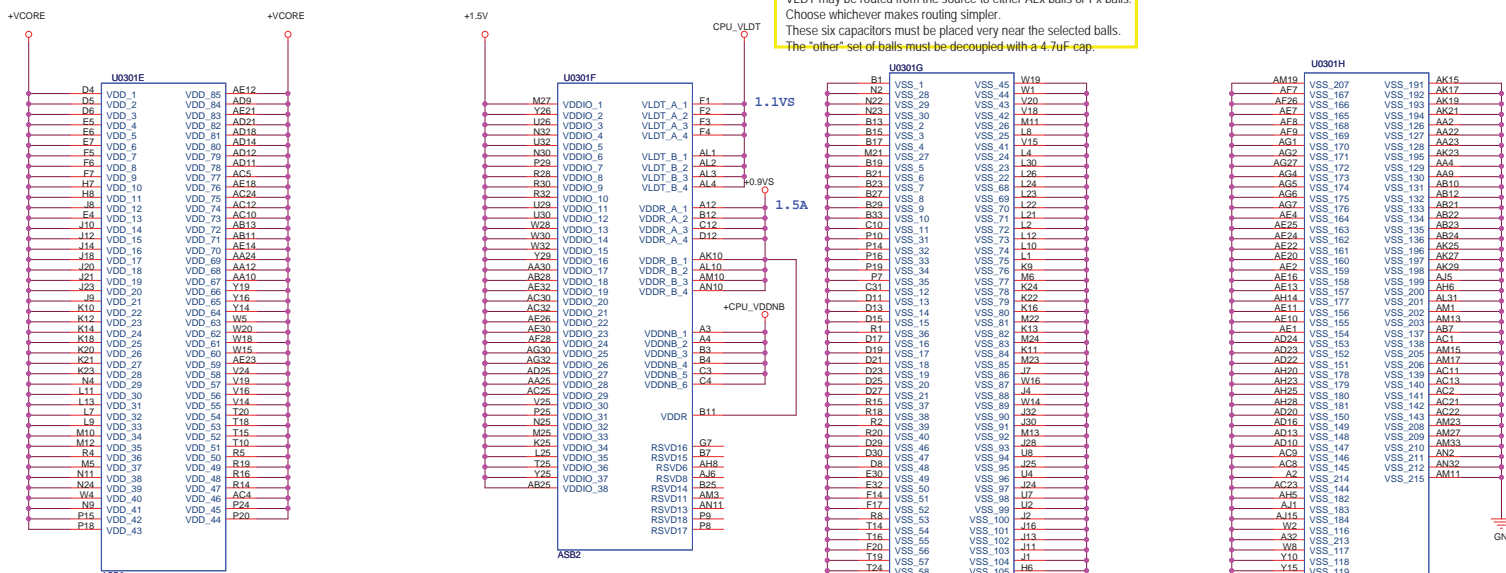
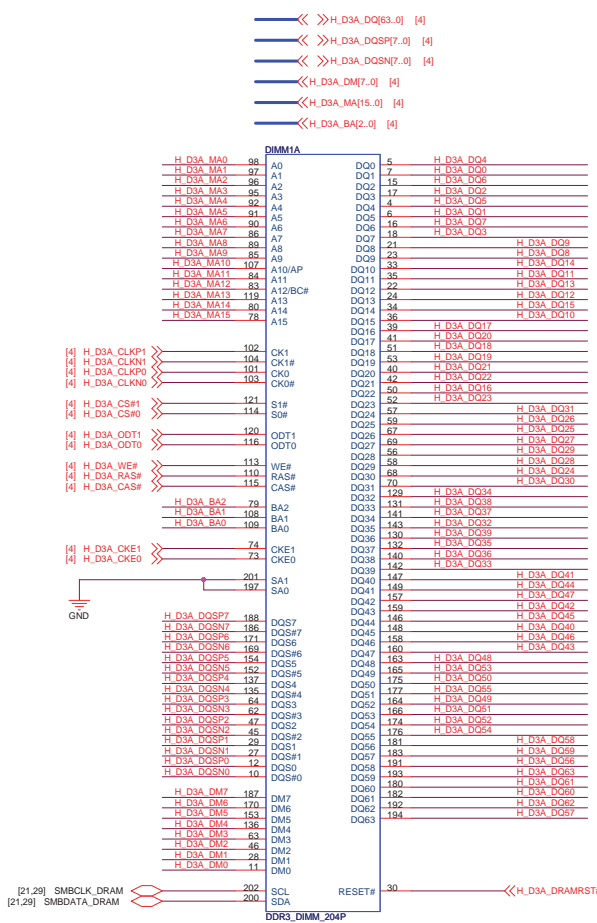


Table 6. Power Supply/Voltage Regulator Interface Pin Descriptions

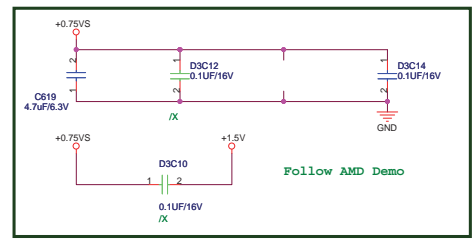
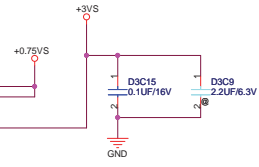
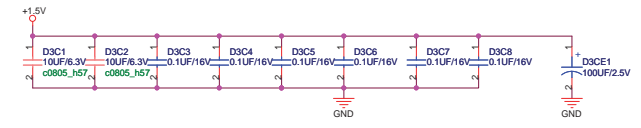
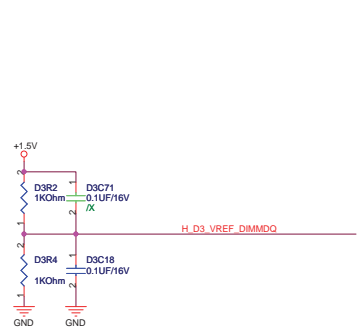
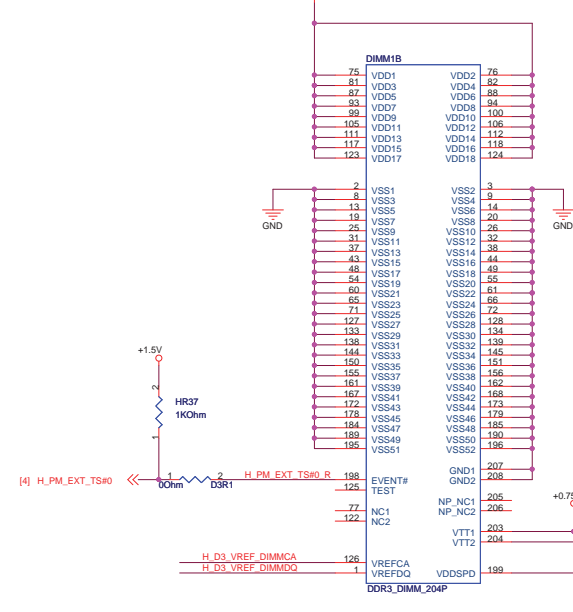
Signal Name	Type	Description
PSI_L	O-I/O-S	Power Status Indicator for the VDD Power Supply regulator. This signal may be used by the regulator to improve efficiency when the processor is in low power states.
VDD	S	Core power supply
VDD_SENSE	A	VDD voltage monitor pin
VDDNB	S	Northbridge power supply
VDDNB_SENSE	A	VDDNB voltage monitor pin
VDDIO	S	DDR SDRAM I/O ring power supply
VDDIO_SENSE	A	VDDIO voltage monitor pin
VDDA	S	Filtered PLL Supply Voltage
VDDR_A_VDDR_B	S	VDDR regulator voltage
VDDR_SENSE	A	VDDR voltage monitor pin
VLDT_A_VLDT_B	S	HyperTransport™ I/O ring power supplies
VLDT_SENSE	A	VLDT voltage monitor pin
VSS	S	Ground
VSS_SENSE	A	VSS voltage monitor pin
SVC	O-I/O-S	Serial VID interface clock
SVC	B-I/O-S	Serial VID interface data

<http://laptop-motherboard-schematic.blogspot.com/>



12G025532043
 12G025532043

R1.1 change DIMM0 to DIMM1



<Variant Name>

ASUS		Title : DDR3 SO-DIMMO	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Date	Rev
C	1215T	Tuesday, August 10, 2010	1.0
Date: Tuesday, August 10, 2010		Sheet 7 of 80	

5

4

3

2

1

D

D

C

C


B

B

A

A

<Variant Name>

		Title : DDR2 SO-DIMM1
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	Rev
Custom	1215T	1.0
Date: Tuesday, August 10, 2010		Sheet 8 of 80

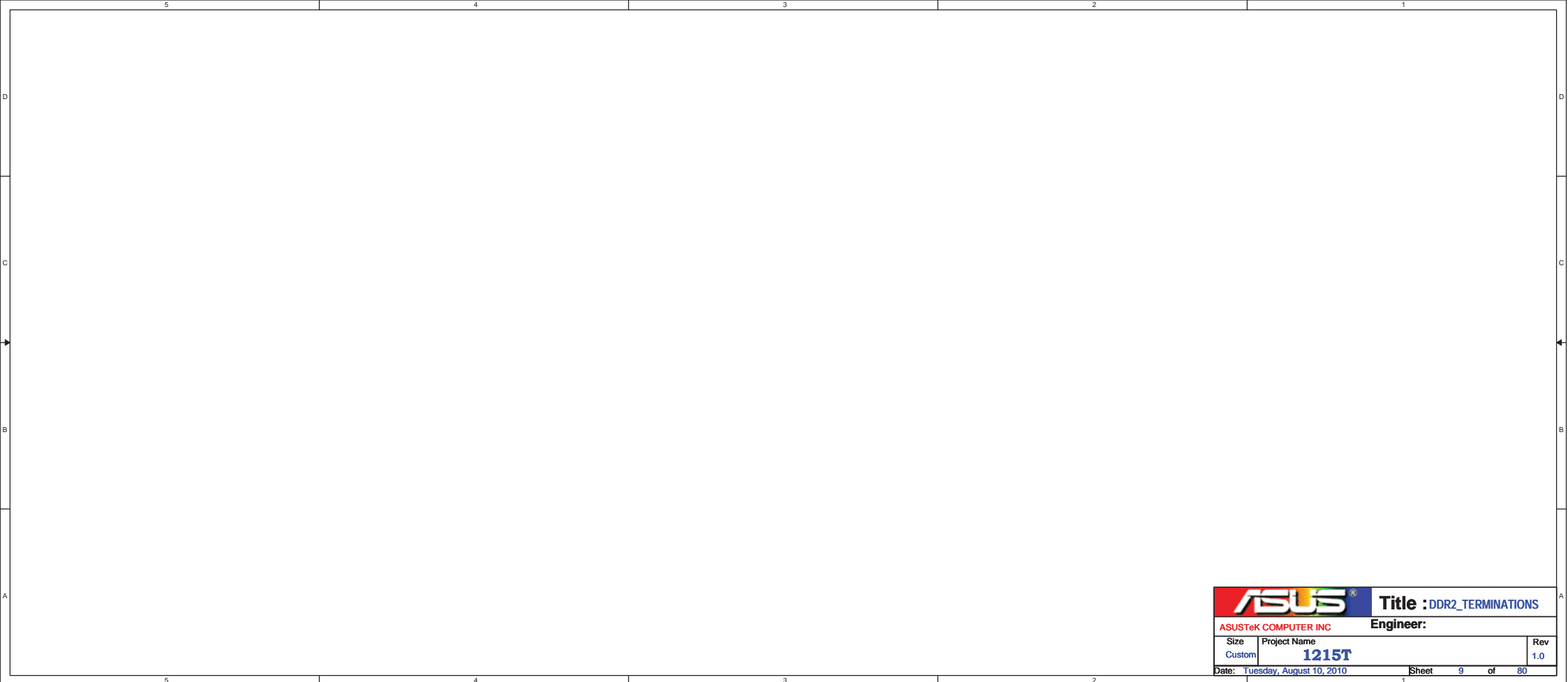
5


4

3

2

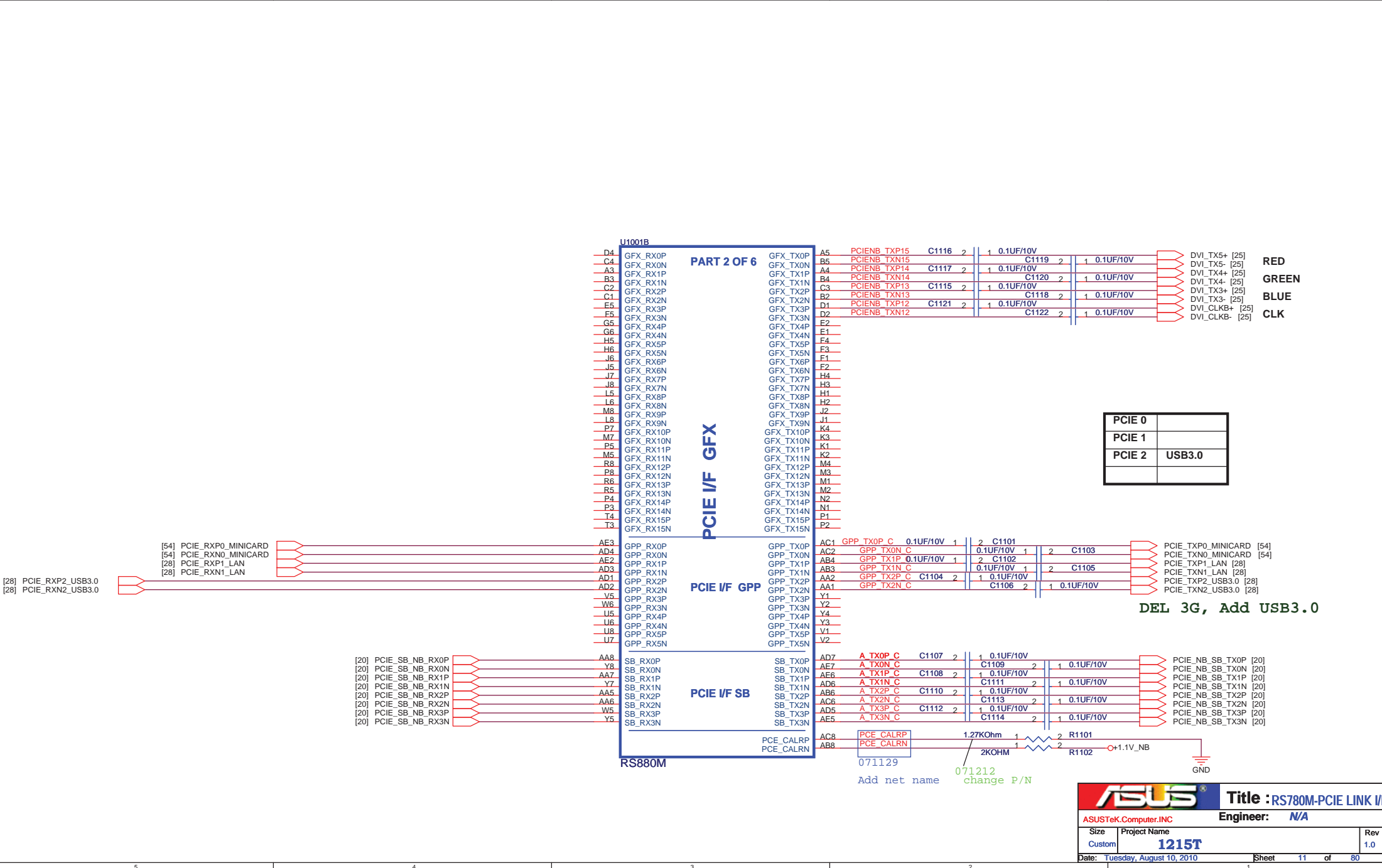
1



		Title : DDR2_TERMINATIONS	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	1215T	1.0	
Date: Tuesday, August 10, 2010		Sheet 9 of 80	

Signal	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP	100R	1.21K	301R
HT_TXCALN			



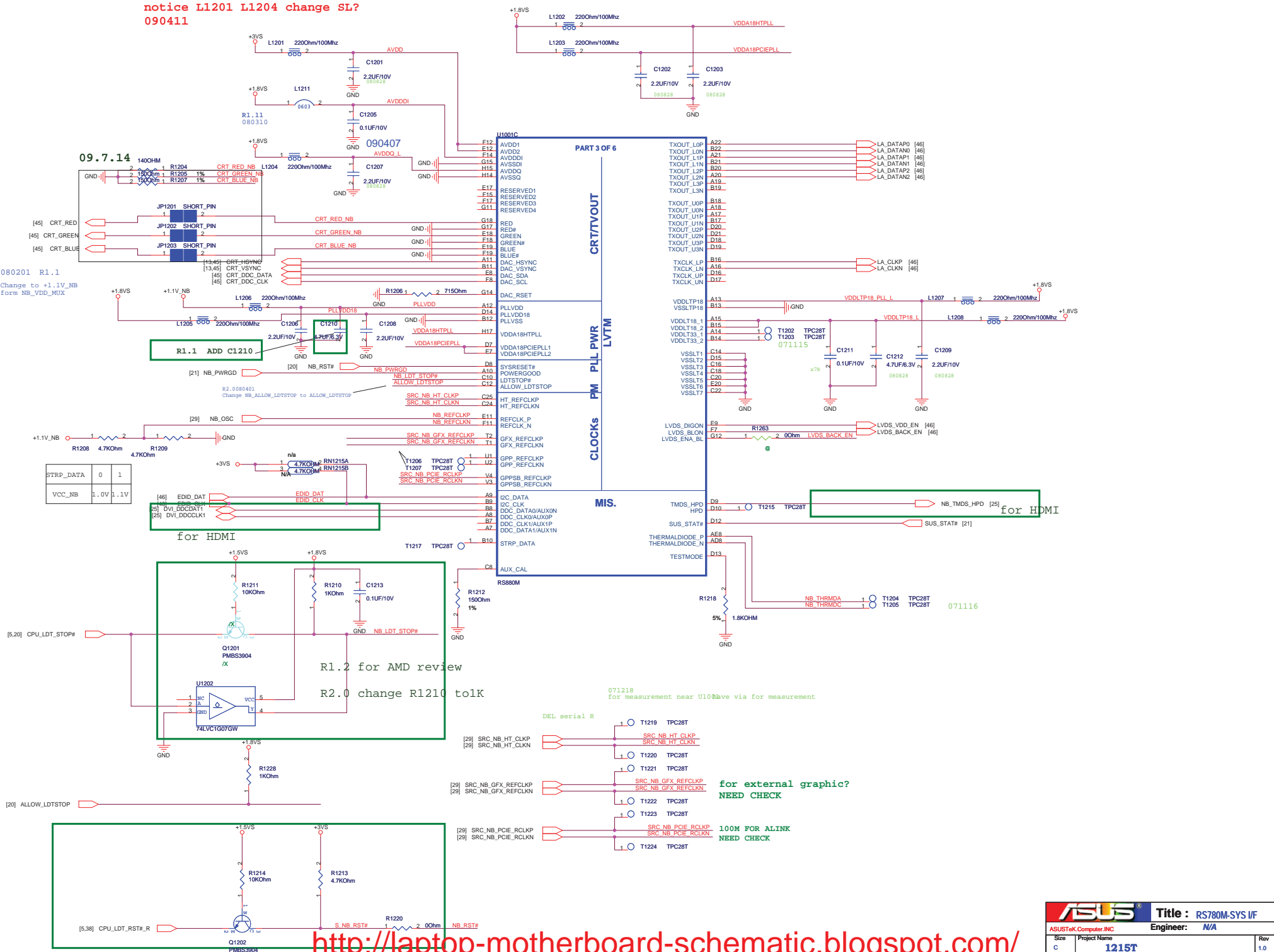


PCIE 0	
PCIE 1	
PCIE 2	USB3.0

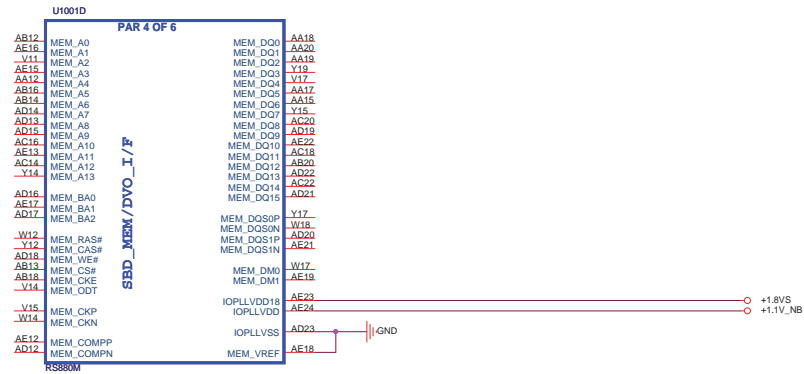
DEL 3G, Add USB3.0

ASUS		Title : RS780M-PCIE LINK I/F	
ASUSTeK.Computer.INC		Engineer: N/A	
Size	Project Name		Rev
Custom	1215T		1.0
Date: Tuesday, August 10, 2010	Sheet	11	of 80

notice L1201 L1204 change SL?
090411



<http://laptop-motherboard-schematic.blogspot.com/>



DFT_GPIO1: LOAD_EEPROM_STRAPS

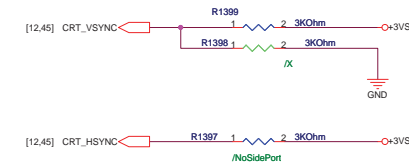
Selects Loading of STRAPS from EPROM
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
 RS780:SUS_STAT

STRAP_DEBUG_BUS_PCIE_ENABLE

Enables the Test Debug Bus using PCIE bus:
 1 : Disable (Can still be enabled using nbcfg register access)
 0 : Enable
 RS780: configurable thru register setting only

RS740/RS780: Enables Side port memory

RS780:HSYNCH#
 Selects if Memory SIDE PORT is available or not
 1 = Memory Side port Not available
 0 = Memory Side port available
 Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

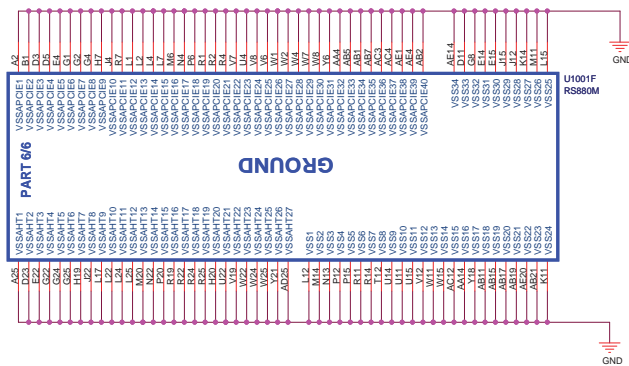
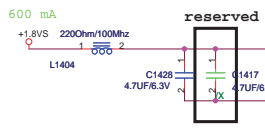
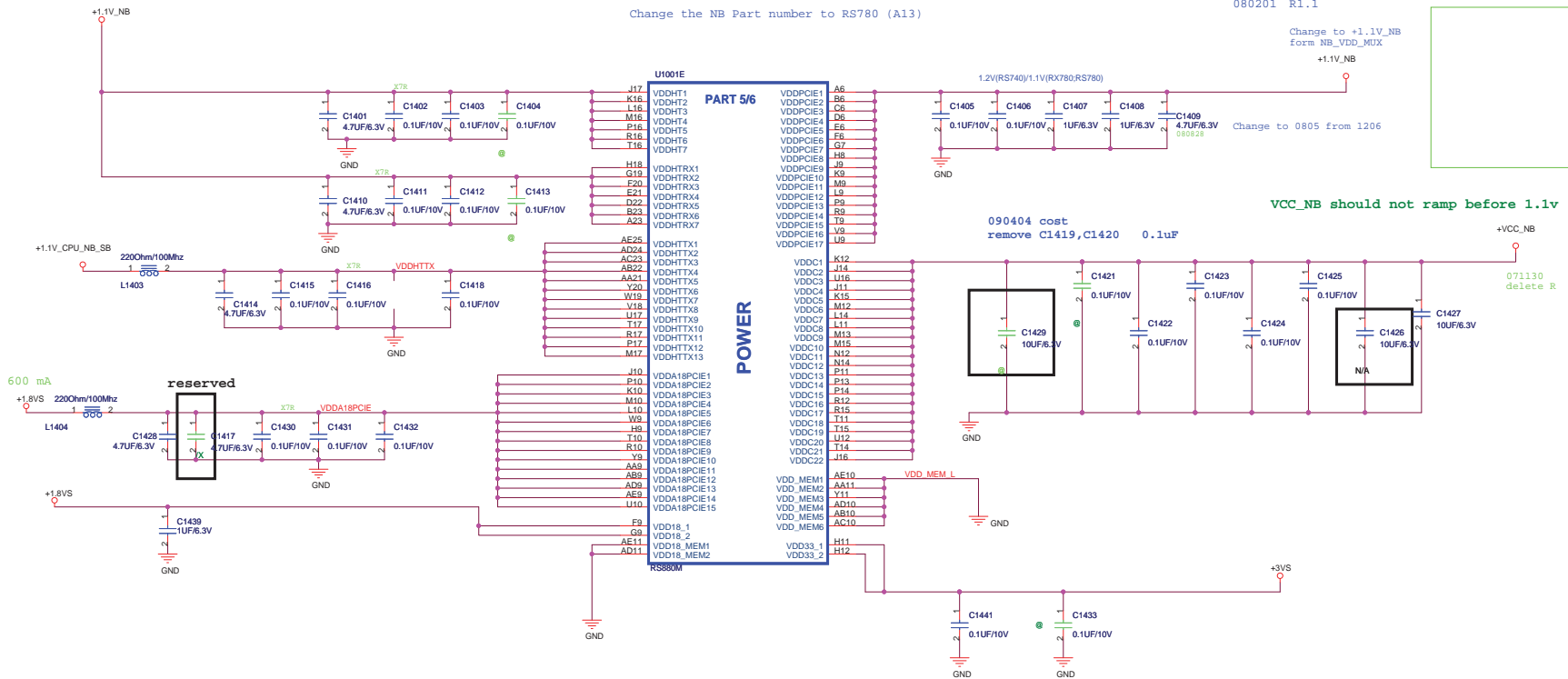


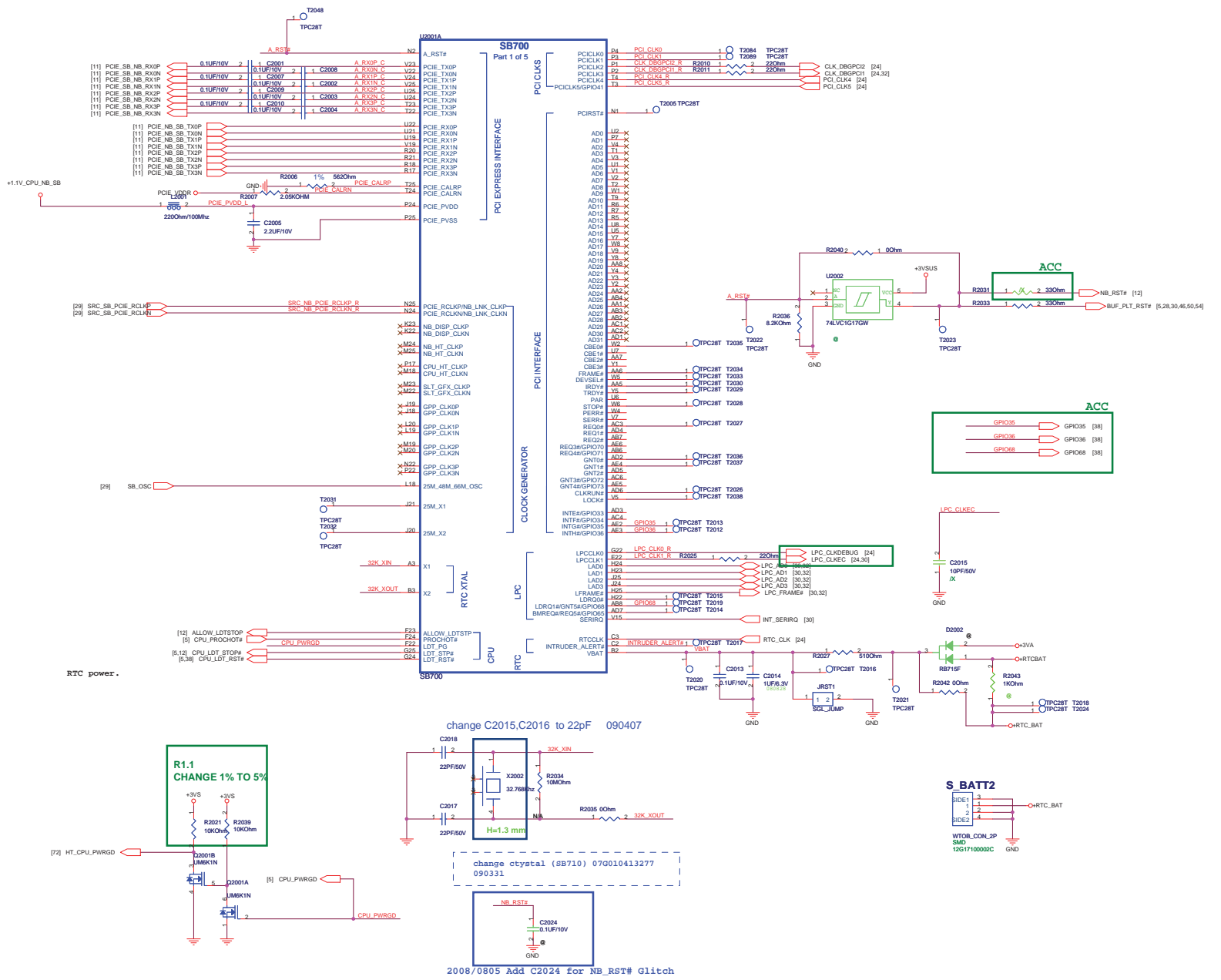
R1.11 080319

Change the NB Part number to RS780 (A13)

080201 R1.1

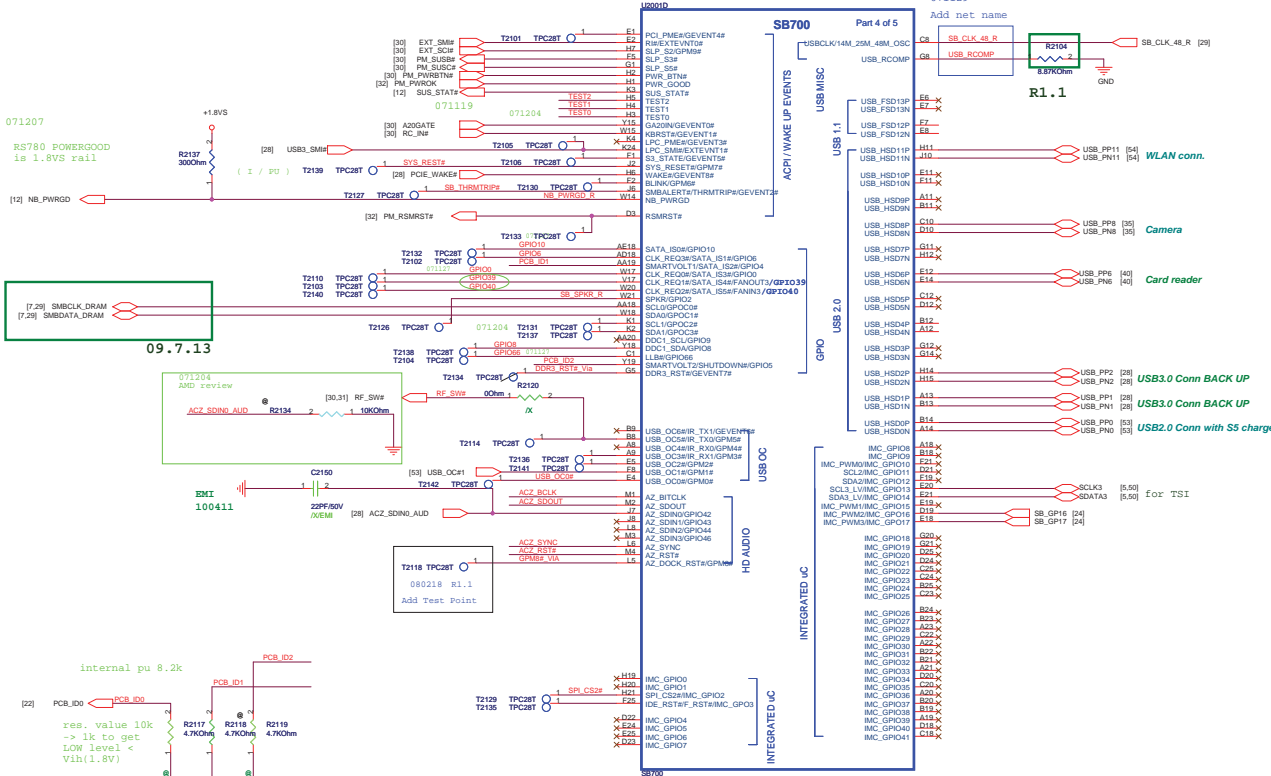
Change to +1.1V_NB
form NB_VDD_MIX



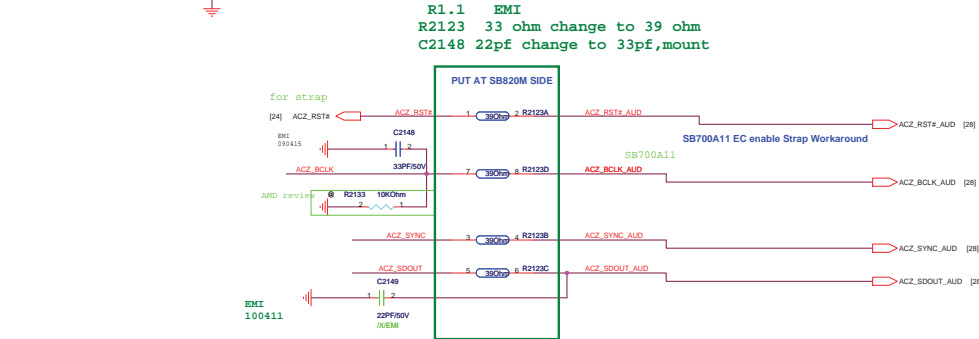
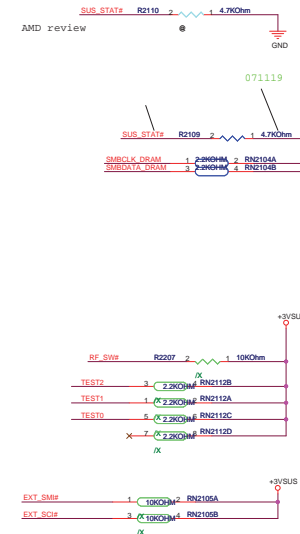


R1.11 080319
Change the SB Part number to SB700 (A12)

071129



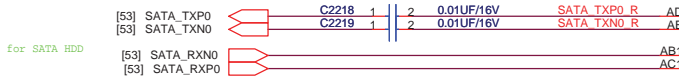
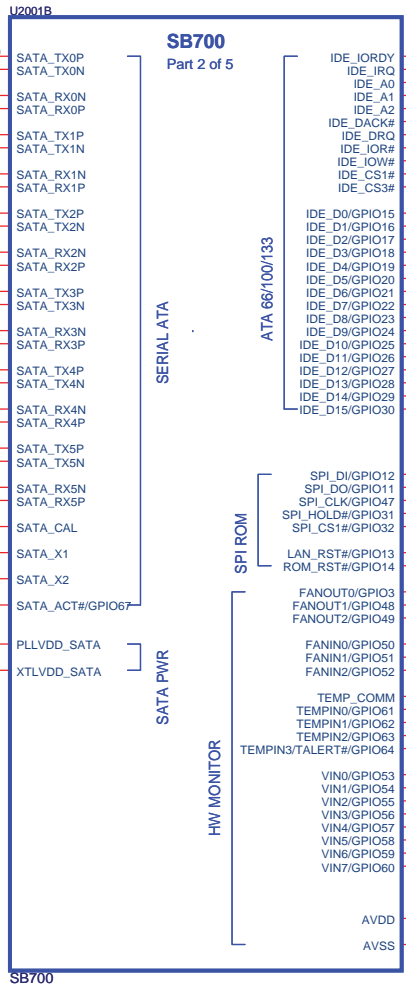
USB 0	External USB
USB 1	External USB
USB 2	
USB 3	
USB 4	
USB 5	
USB 6	Card reader
USB 7	
USB 8	CAMERA
USB 9	
USB 10	
USB 11	WLAN(MiniCard)
USB 12	
USB 13	
USB 14	
USB 15	



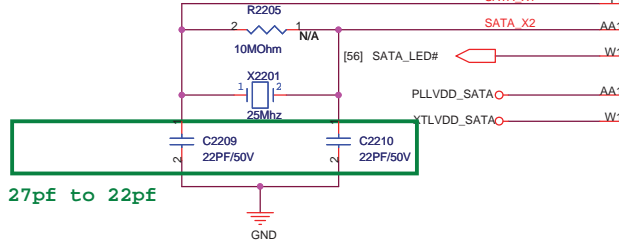
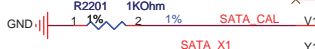
R1.1 EMI
R2123 33 ohm change to 39 ohm
C2148 22pf change to 33pf, mount

PUT AT SB820M SIDE

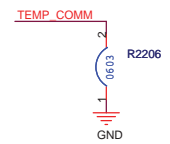
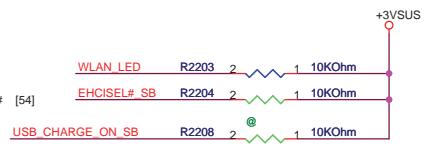
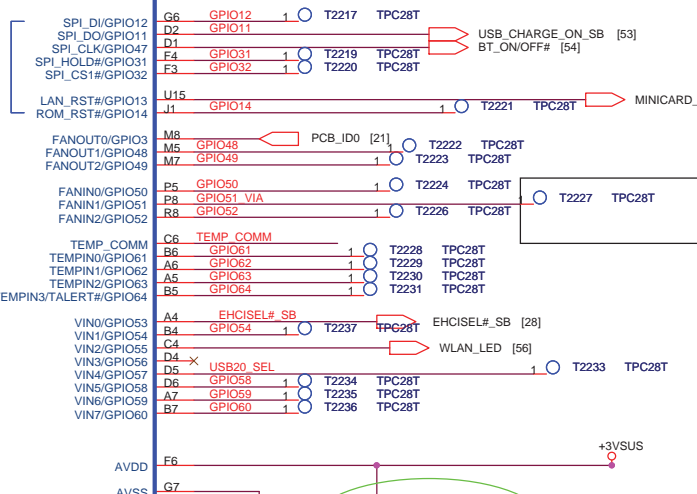
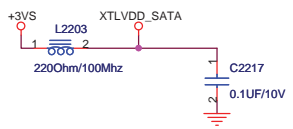
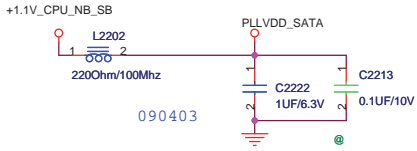
Change the SB Part number to SB710 (A14)



Place SATA_CAL RES very close to ball of SB700



R1.1 change 27pf to 22pf



HWM not Implemented: Decoupling caps not used. 071119

GND trace at least 10mil wide

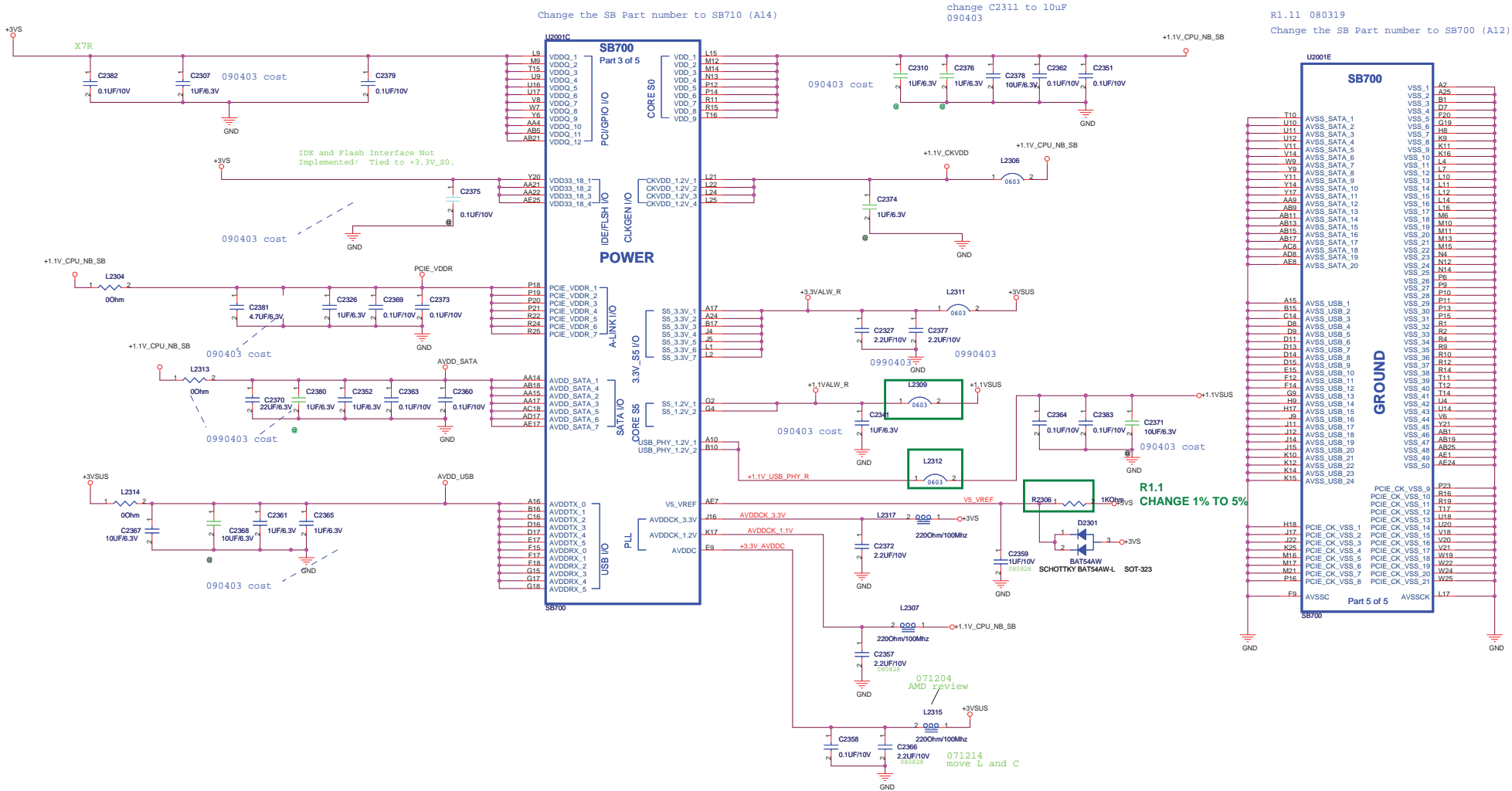
<Variant Name>

ASUS Title: SB700_PATA/SATA

ASUSTeK Computer, INC Engineer: N/A

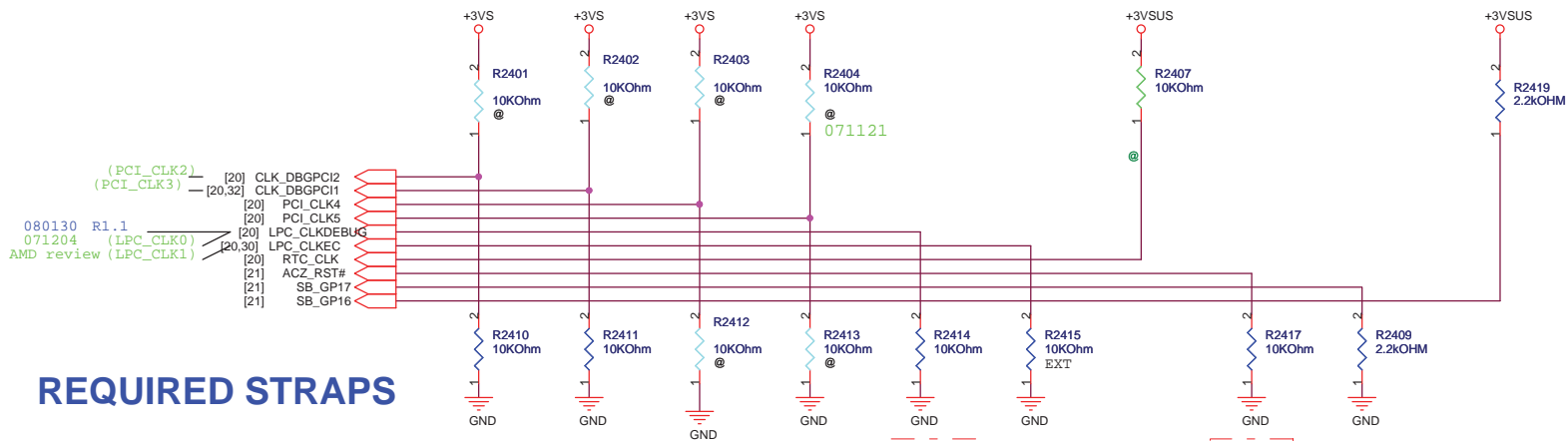
Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 22 of 80



Remove R2405, R2406, R2416
R2408, R2418, R2420, R2418 090405

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI MEM BOOT	H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM	

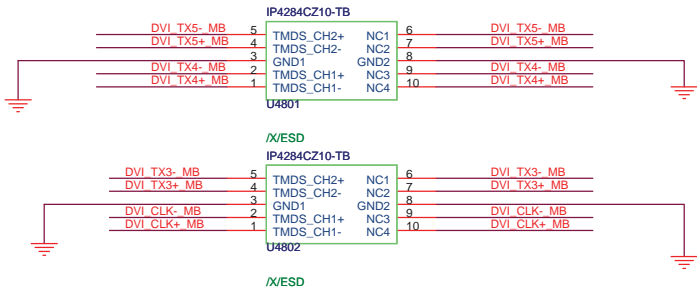
For SB700 A12 and later version

080204 R1.1
Change the Text Comment

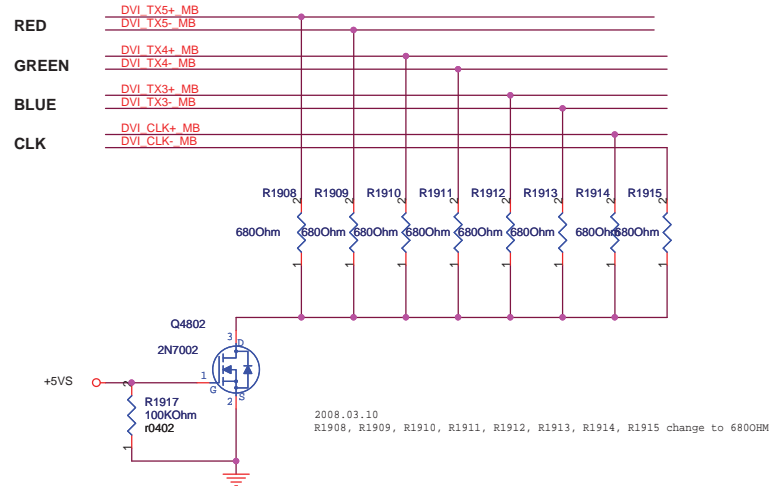
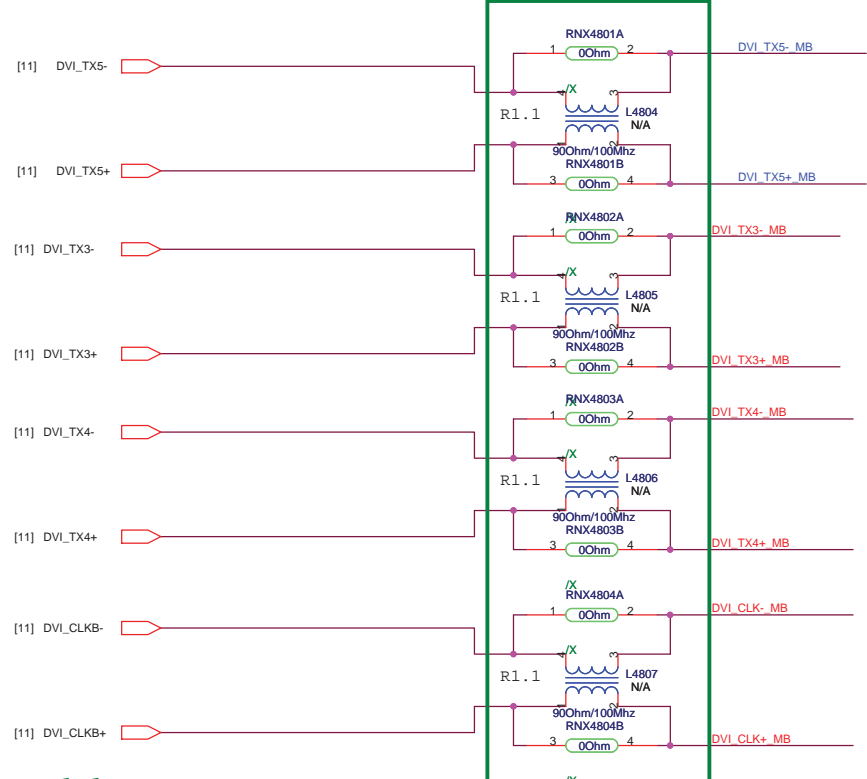
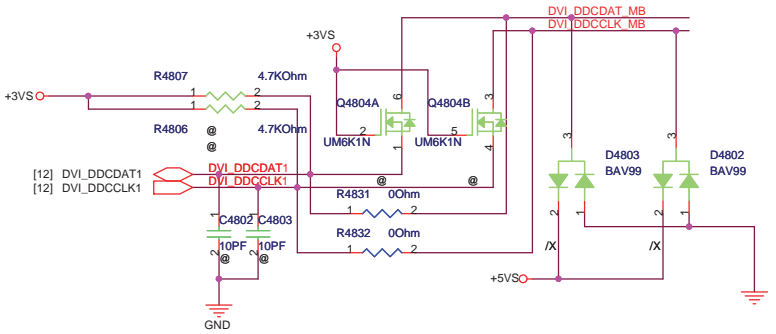
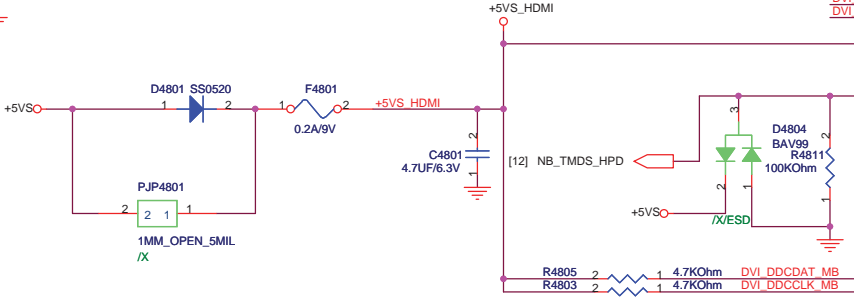
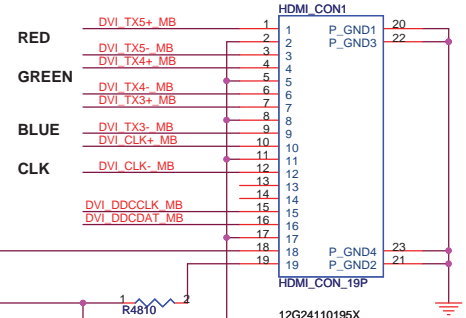
<Variant Name>

ASUS		Title : SB700_STRAP	
ASUSTeK Computer, INC		Engineer: N/A	
Size	Project Name		Rev
Custom	1215T		1.0
Date: Tuesday, August 10, 2010		Sheet	24 of 80

Close to HDMI CON(ESD Protection)



HDMI CON



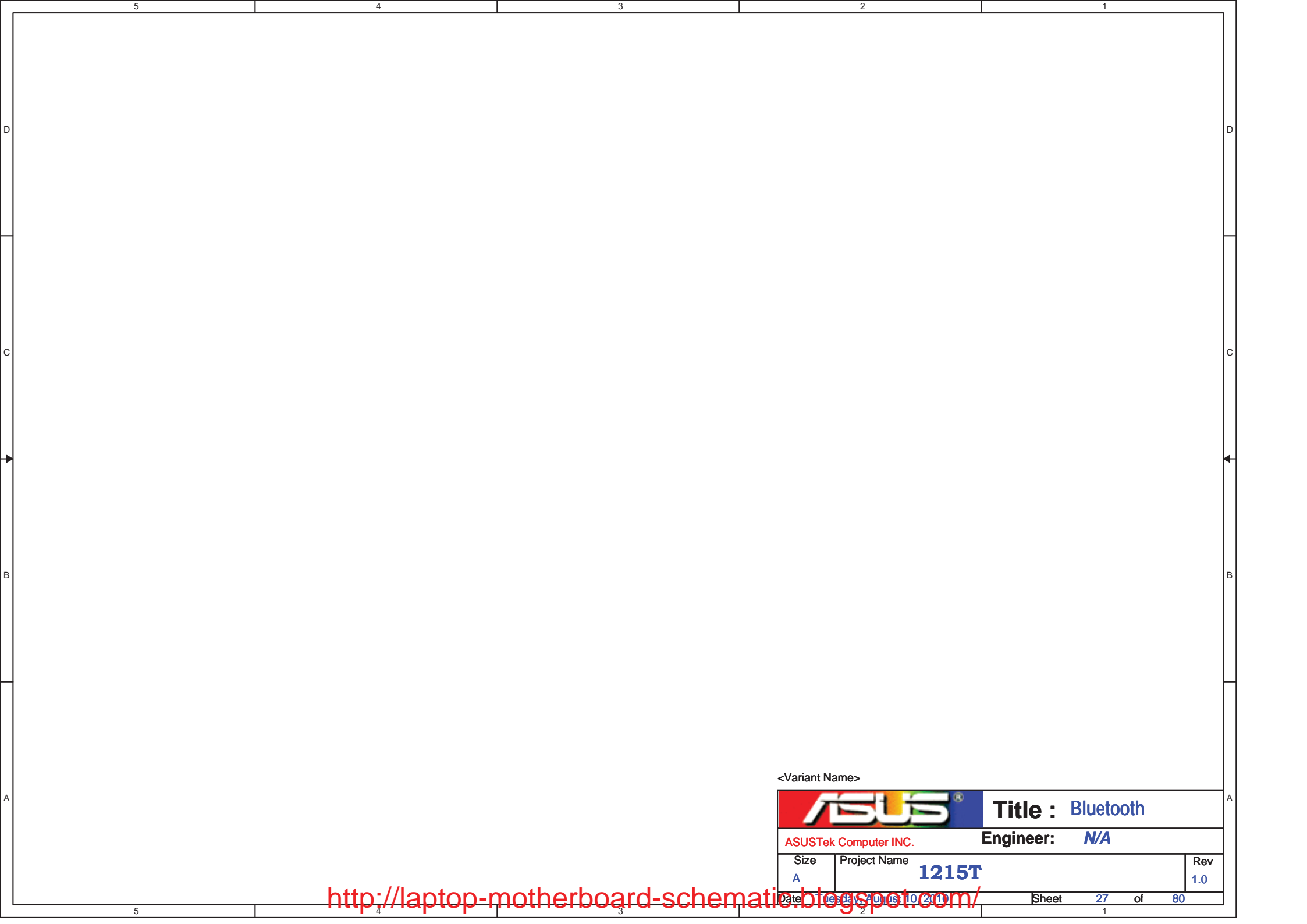
R1.1 EMI
mount choke, unmount 0 ohm resistor

2008.03.10
R1908, R1909, R1910, R1911, R1912, R1913, R1914, R1915 change to 680OHM


<Variant Name>

ASUS Title : HDMI
ASUSTek COMPUTER INC Engineer: N/A

Size	Project Name	Rev
Custom	1215T	1.0
Date: Tuesday, August 10, 2010	Sheet	25 of 80

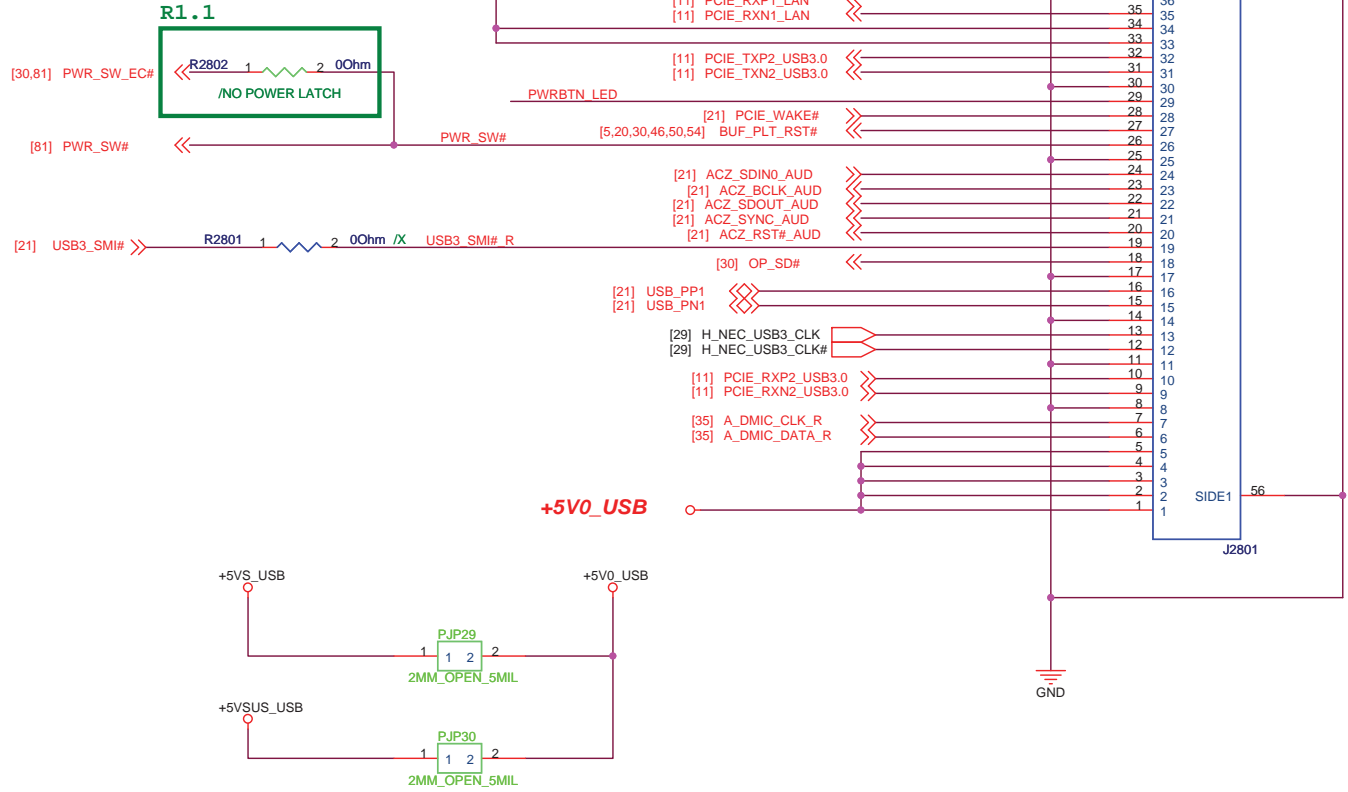
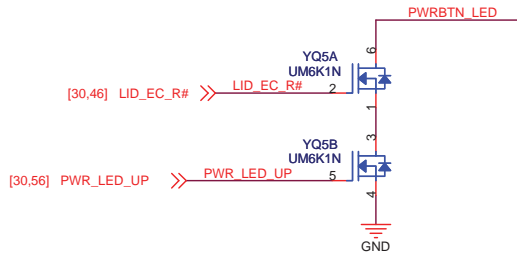


<Variant Name>

		Title : Bluetooth
ASUSTek Computer INC.		Engineer: N/A
Size A	Project Name 1215T	Rev 1.0
Date Wednesday, 10/20/10	Sheet 27	of 80

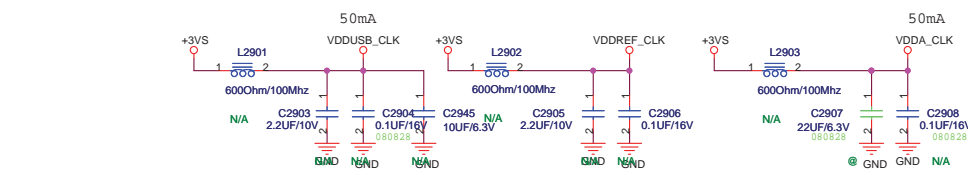
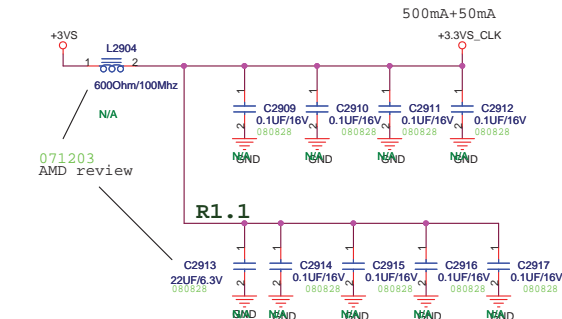
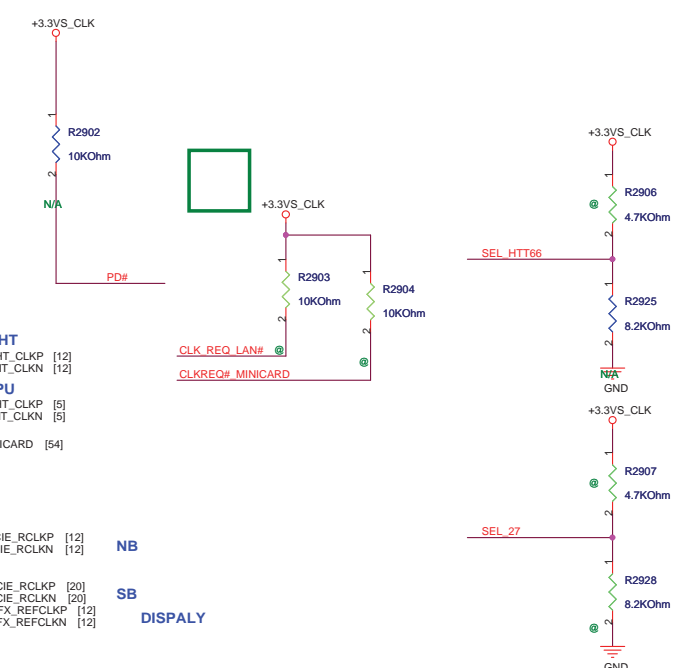
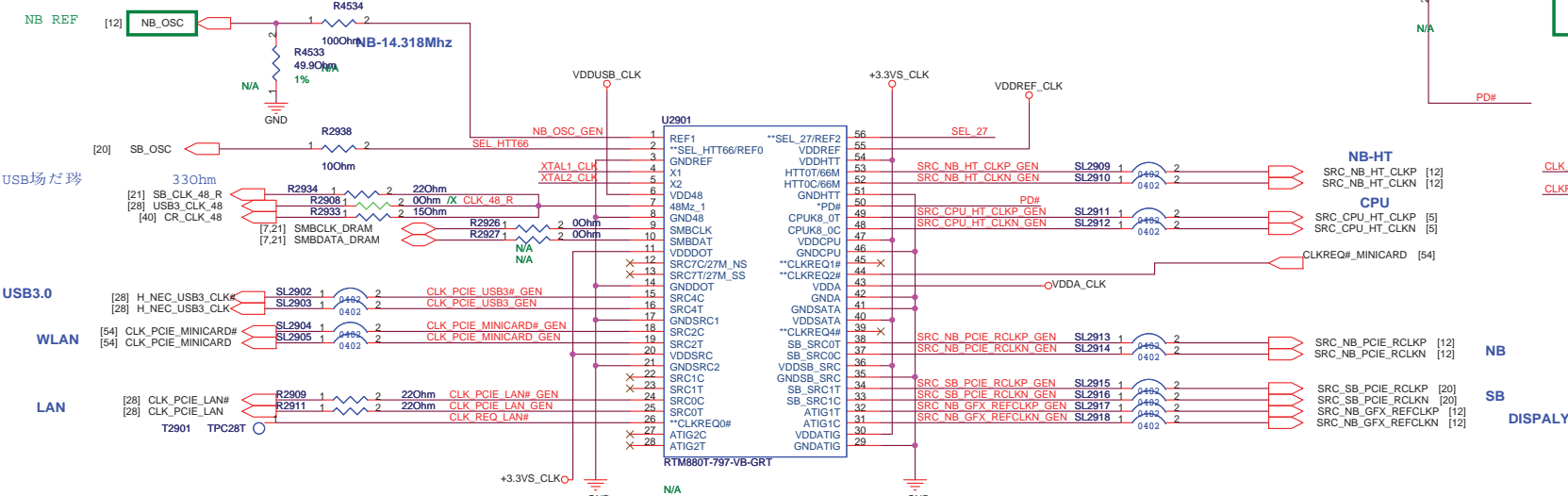
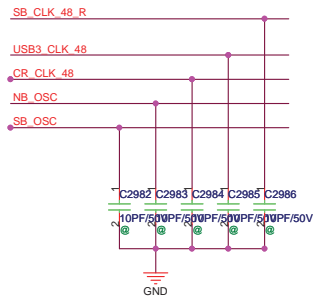
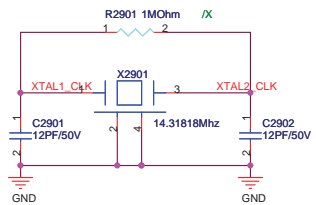
<http://laptop-motherboard-schematic.blogspot.com/>

5/20, Swap Pin15,16 and 42,43, follow 1215N



<Variant Name>		ASUS		Title : Small brd Conn	
ASUSTek Computer INC.		Engineer: N/A			
Size	Project Name			Rev	
B	1215T			1.0	
Date: Tuesday, August 10, 2010		Sheet 28 of 80			

Change to small One, follow 1018P



SEL_27	0	100 MHz differential spreading SRC clock
	1	27MHz non-spreading singled clock on pin12 27MHz spread clock on pin13.

SEL_HTT66	0	100 MHz differential HTT clock
	1	66MHz 3.3V single ended HTT clock

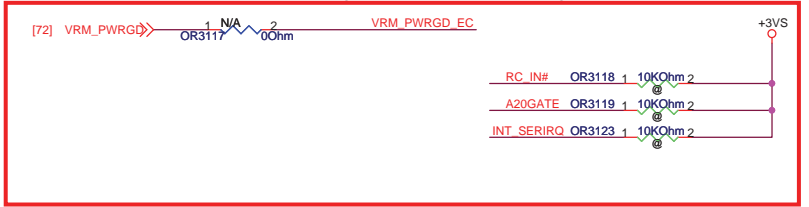
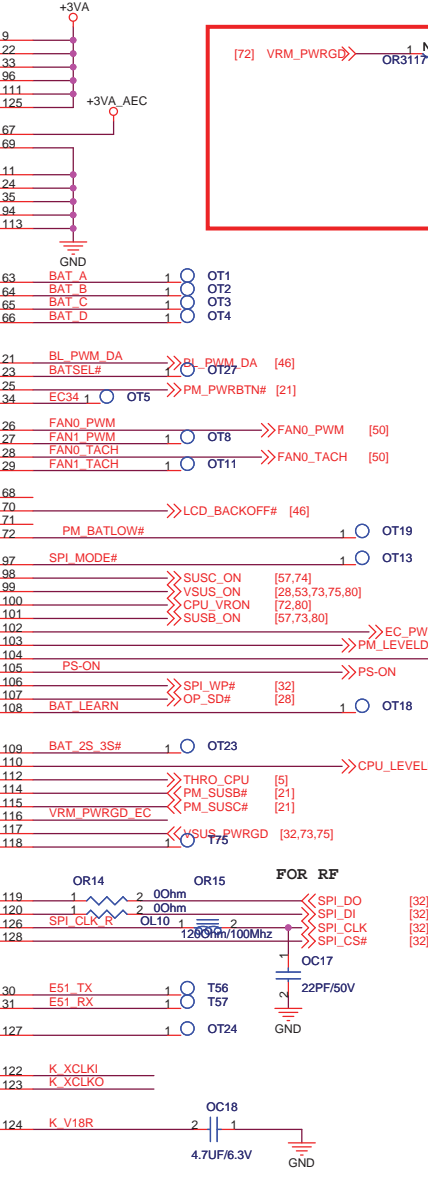
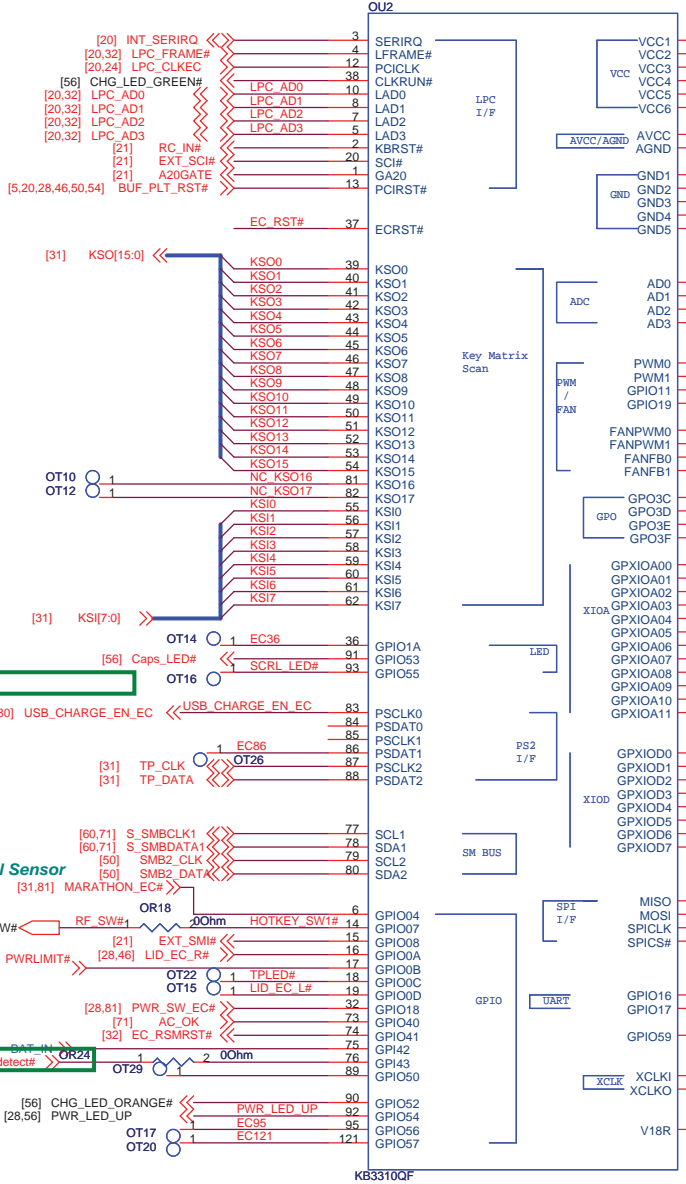
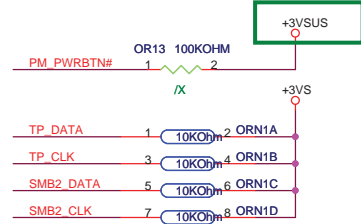
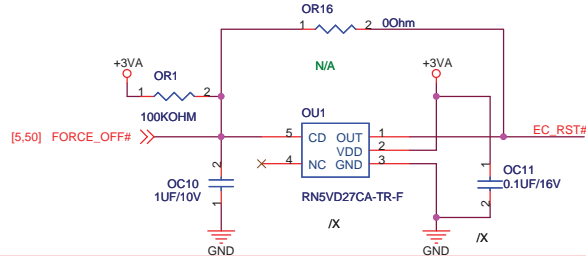
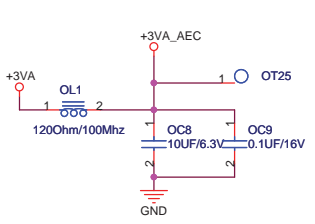
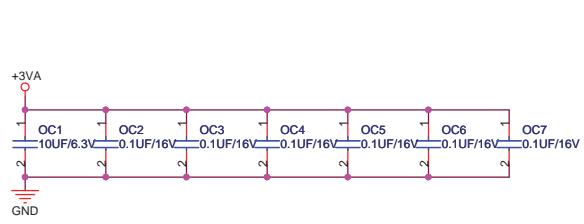
<Variant Name>

ASUS Title: RTM880T-797-VB-GRT

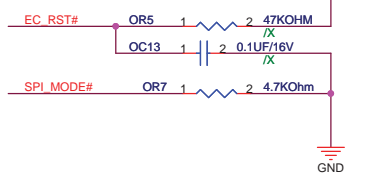
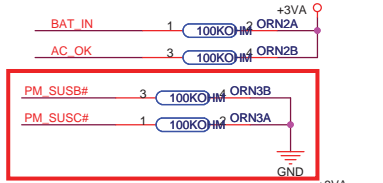
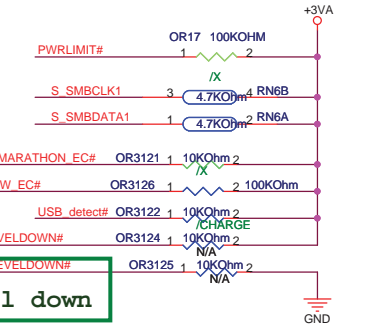
ASUSTeK COMPUTER INC Engineer: N/A

Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 29 of 80

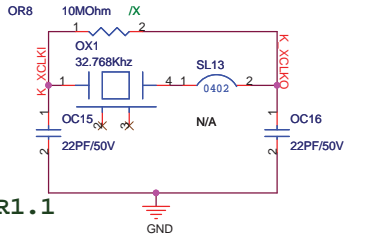
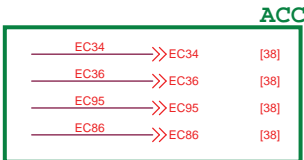


R1.1 change to pull down



Hotkey Table

Item	Pin Name	Function
0	HOTKEY_SW0#	Home



<Variant Name>



ASUSTek Computer INC. Engineer: N/A

Size: A3 Project Name: 1215T Rev: 1.0

Date: Tuesday, August 10, 2010 Sheet: 30 of 80

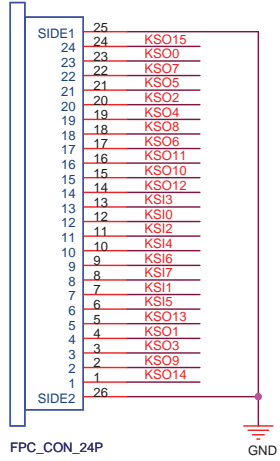
HOTKEY_SW0# - HOTKEY_SW3# internal PU

<http://laptop-motherboard-schematic.blogspot.com/>

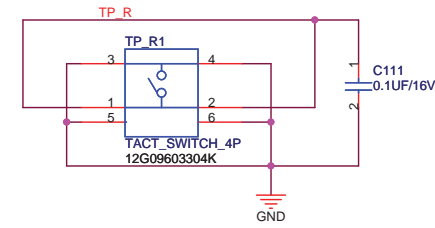
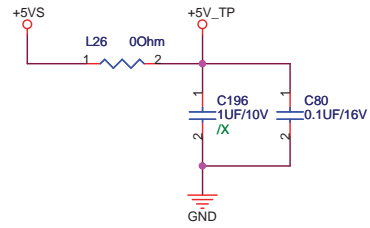
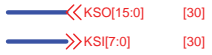
02G890000712 VER: C1

follow 1201T

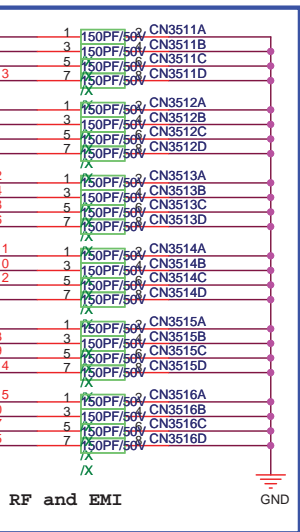
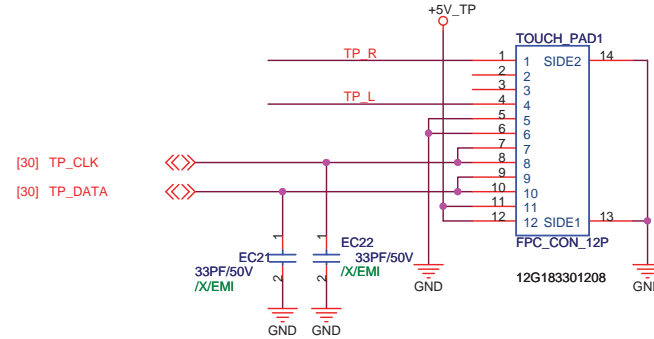
KB_CON1 12G182102402



For Keyboard Connector

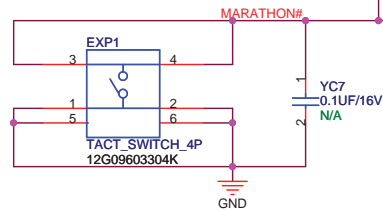
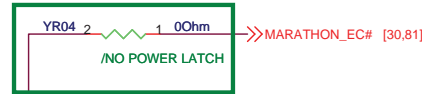


For Touch-Pad



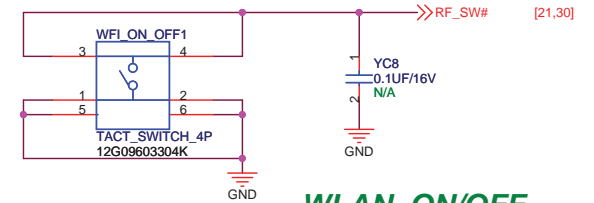
FOR RF and EMI

R1.1



EXPRESS GATE & SHE

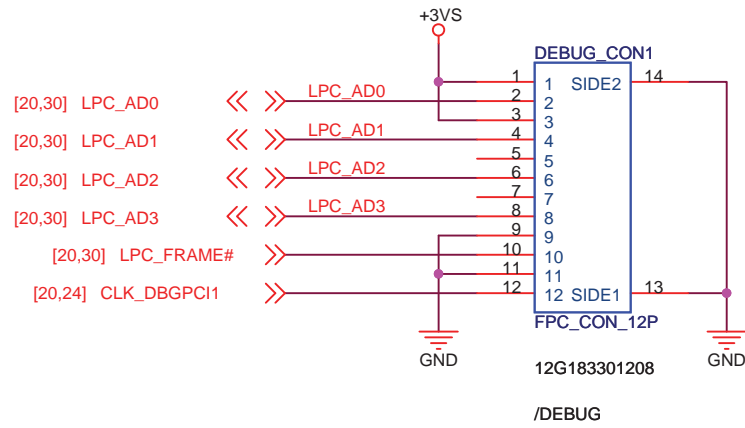
**R1.1
DEL PWR1**



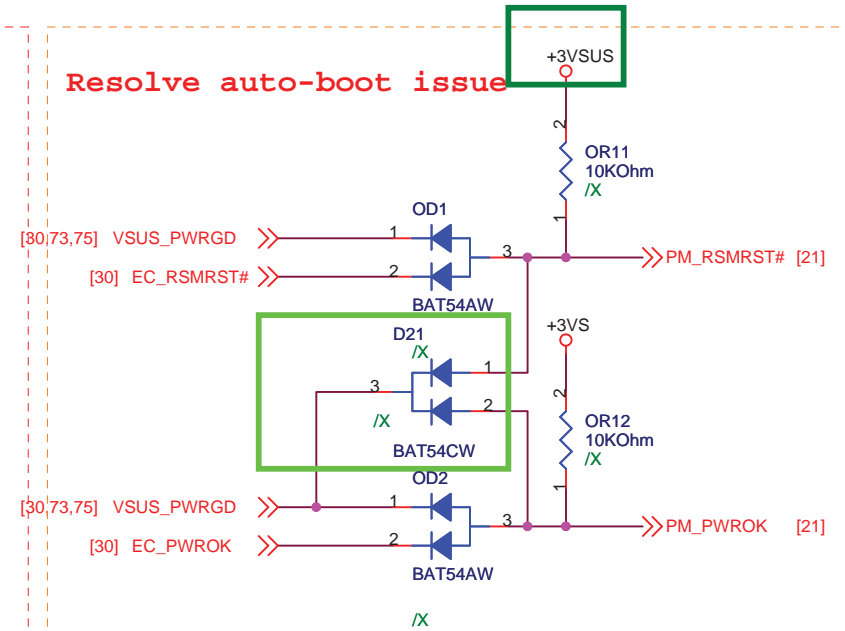
WLAN_ON/OFF

ASUS		Title : KB_Touch Pad	
ASUSTek Computer INC.		Engineer: N/A	
Size	Project Name		Rev
B	1215T		1.0
Date: Tuesday, August 10, 2010		Sheet 31 of 80	

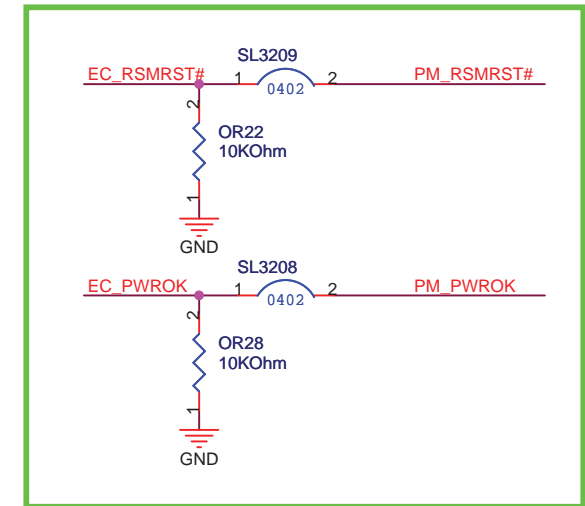
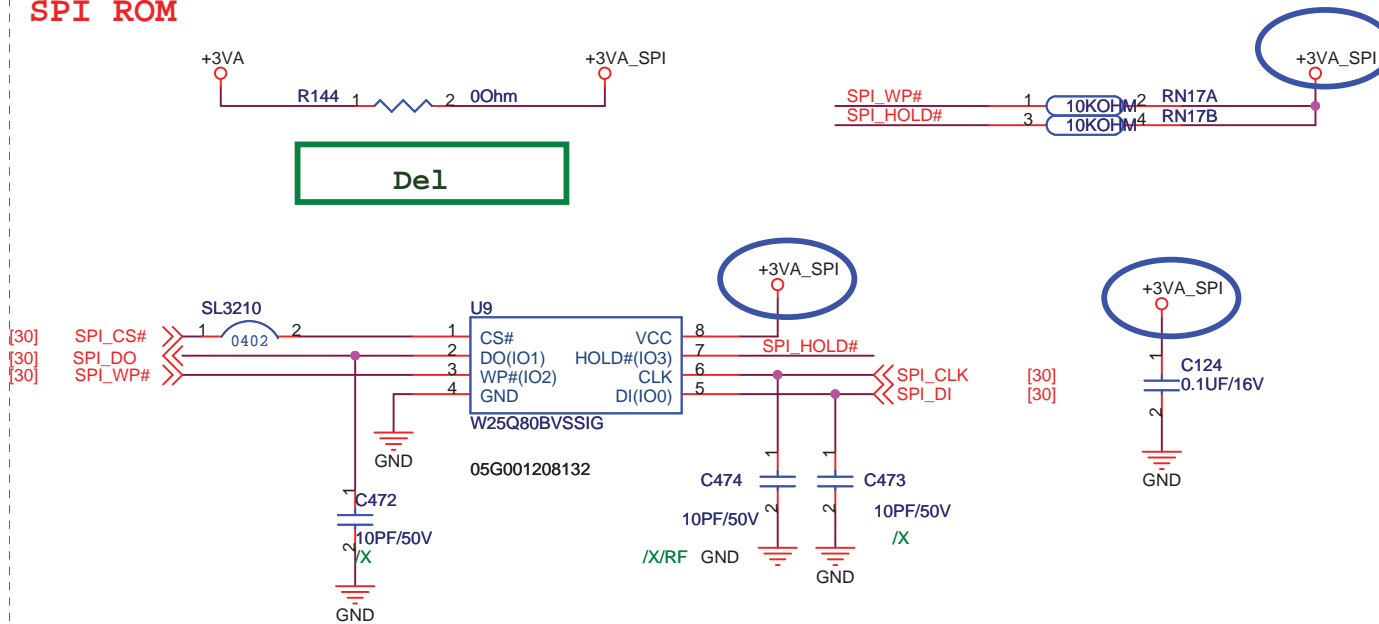
For Debug



Resolve auto-boot issue



SPI ROM



<Variant Name>

ASUS		Title : SPI ROM/ Debug	
ASUSTek Computer INC.		Engineer: N/A	
Size A4	Project Name 1215T	Rev 1.0	
Date: Tuesday, August 10, 2010	Sheet 32		of 80

5

4

3

2

1

D

D

C

C


B

B

A

A

<http://laptop-motherboard-schematic.blogspot.com/>

<Variant Name>		
		
Title : AR8113/AR8132		
ASUSTek Computer INC Engineer: N/A		
Size	Project Name	Rev
A3	1215T	1.0
Date: Tuesday, August 10, 2010		Sheet 33 of 80

5

4

3

2

1

D

D

C

C

B

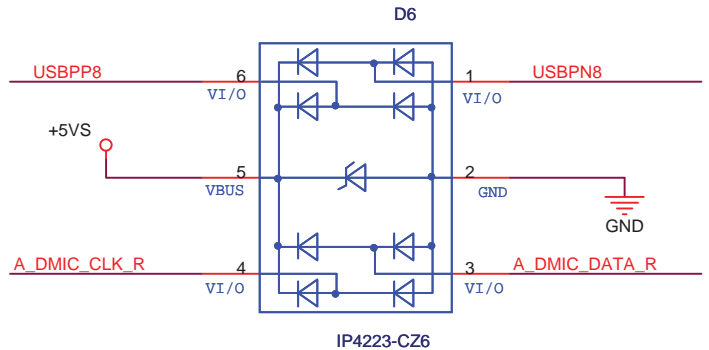
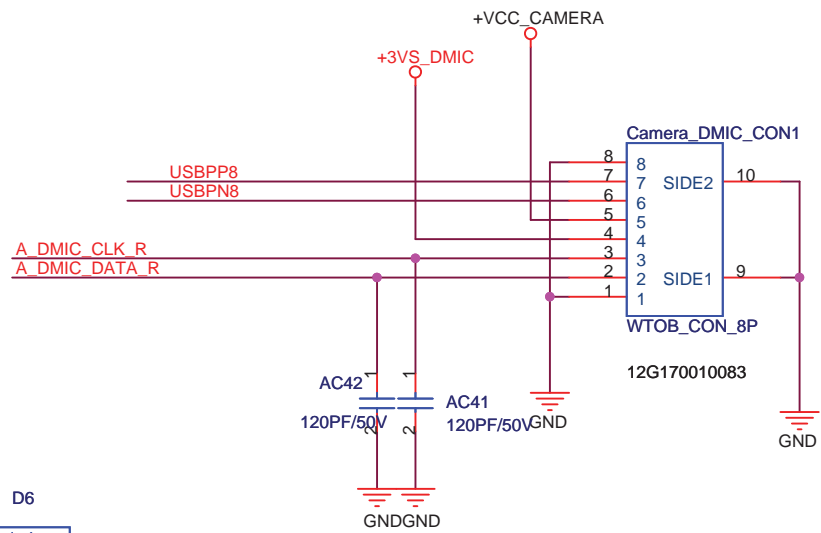
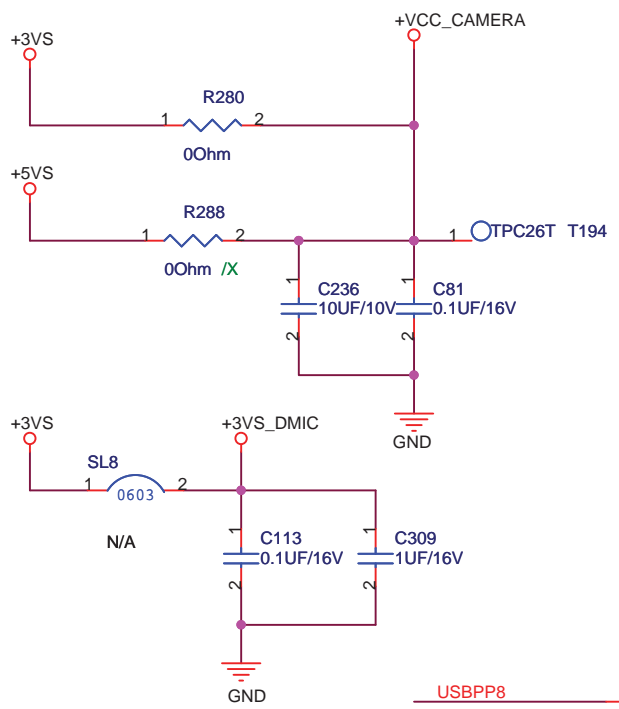
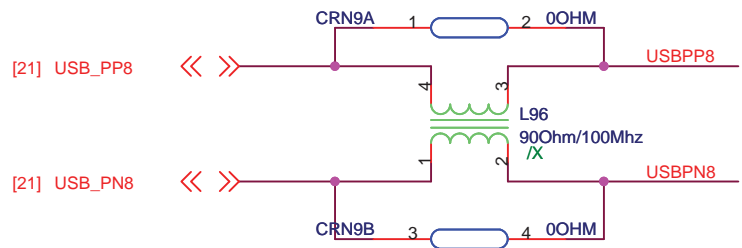
B

A

A

<http://laptop-motherboard-schematic.blogspot.com/>

<Variant Name>		
 Title : RJ45		
ASUSTek Computer INC. Engineer: N/A		
Size A3	Project Name 1215T	Rev 1.0
Date: Tuesday, August 10, 2010		Sheet 34 of 80



<Variant Name>

ASUS		Title : CMOS	
ASUSTek Computer INC.		Engineer: N/A	
Size	Project Name	Rev	
A4	1215T	1.0	
Date:	Tuesday, August 10, 2010	Sheet	35 of 80


<http://laptop-motherboard-schematic.blogspot.com/>

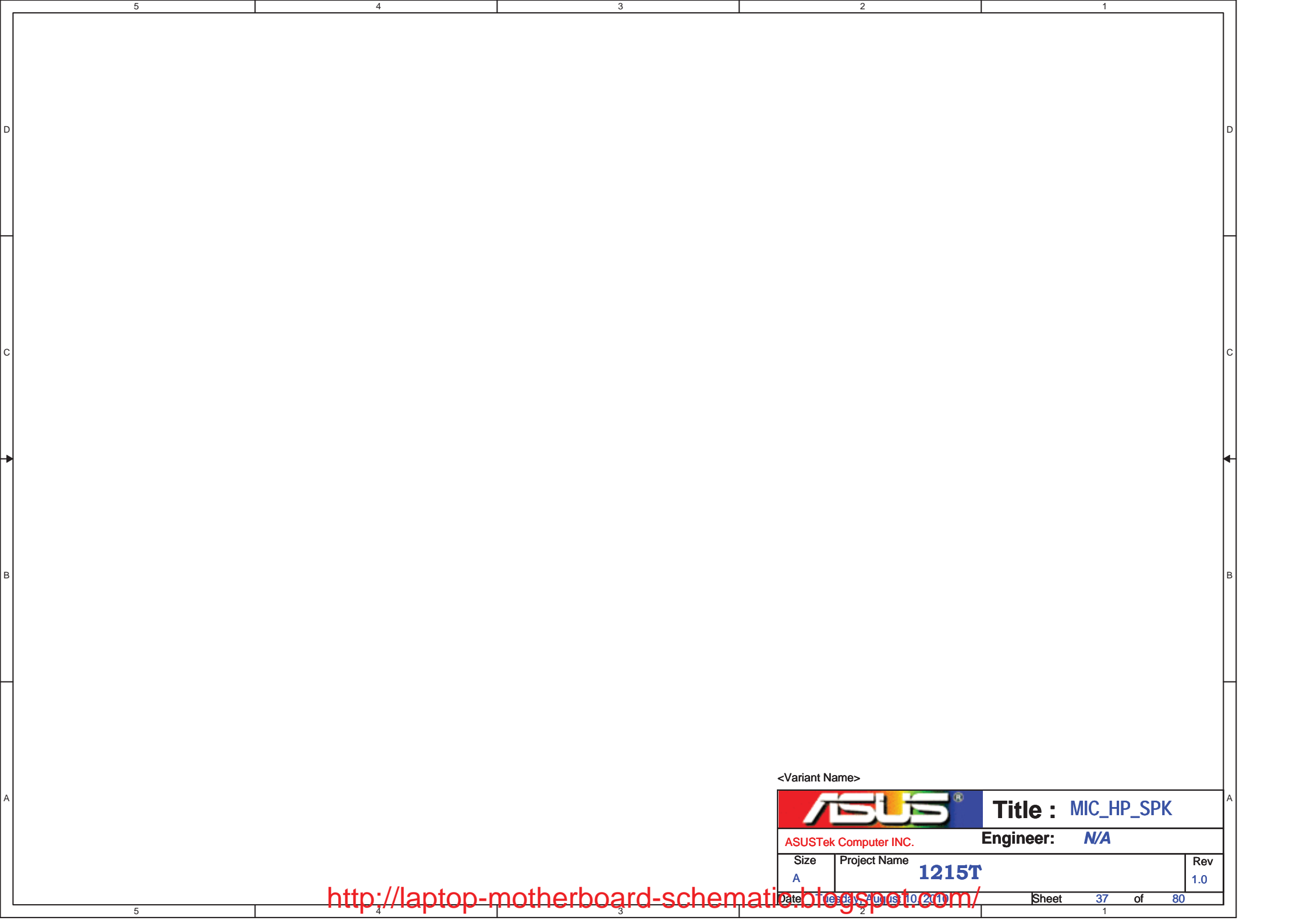
NOTE

VA6:02G611005006


VB5:02G611005015

<Variant Name>

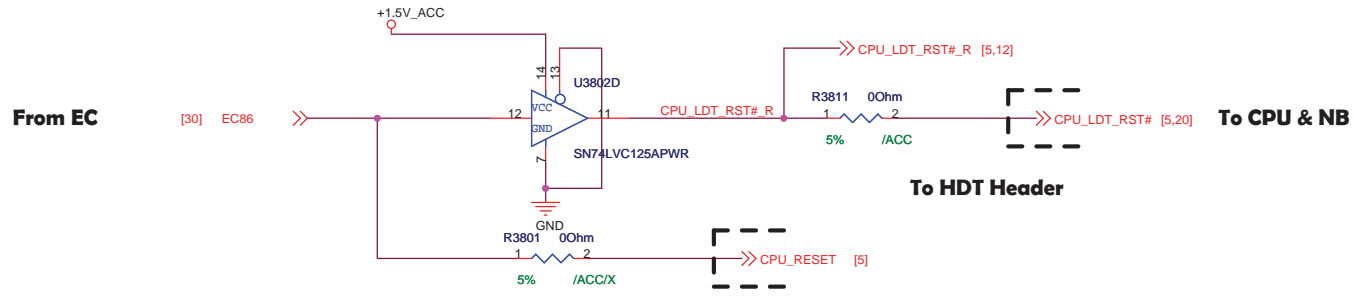
		Title : ALC269
ASUSTek Computer INC.		Engineer: N/A
Size A	Project Name 1215T	Rev 1.0
Date Wednesday, 10/20/10	Sheet 36	of 80



<Variant Name>

		Title : MIC_HP_SPK
ASUSTek Computer INC.		Engineer: N/A
Size A	Project Name 1215T	Rev 1.0
Date Wednesday, 10/20/10	Sheet 37	of 80

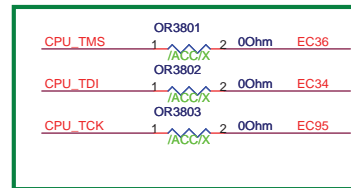
AOD ACC Function



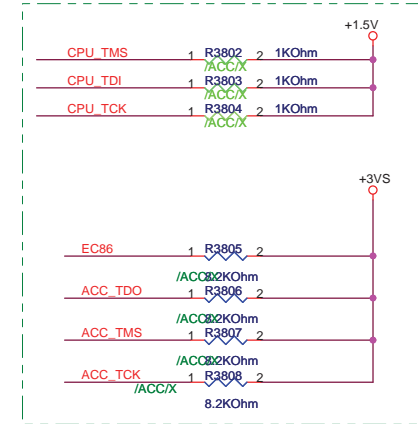
Connect with CPU Debug Port

- [5] CPU_TMS <<
- [5] CPU_TDI <<
- [5] CPU_TCK <<

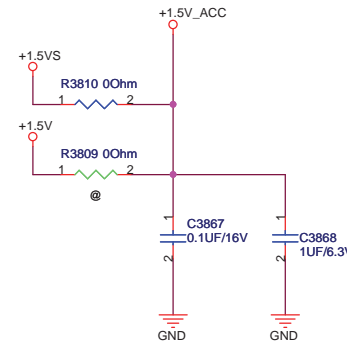
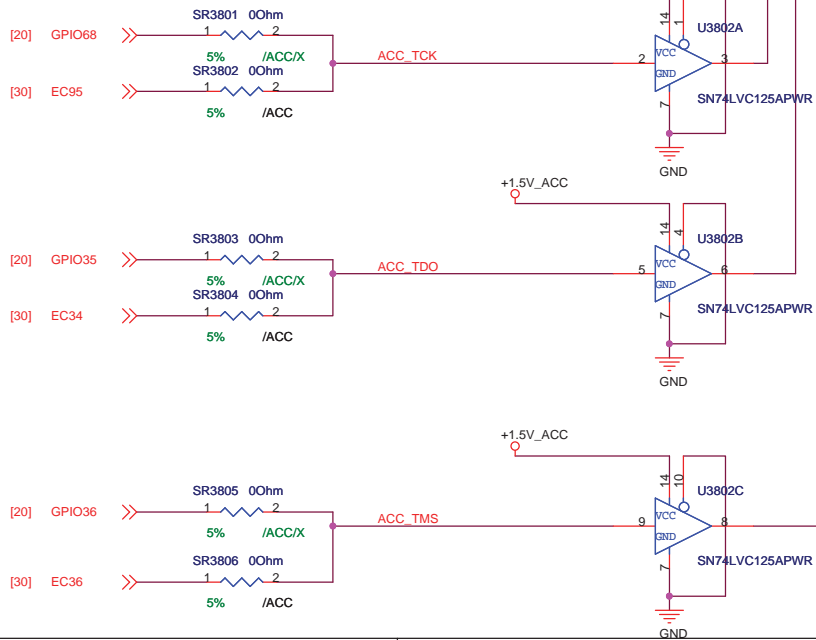
EC Direct Route



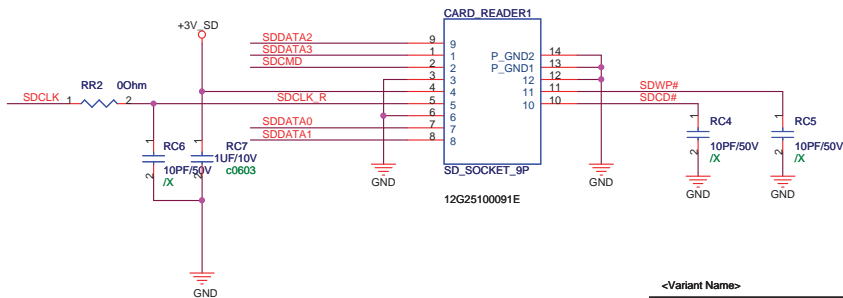
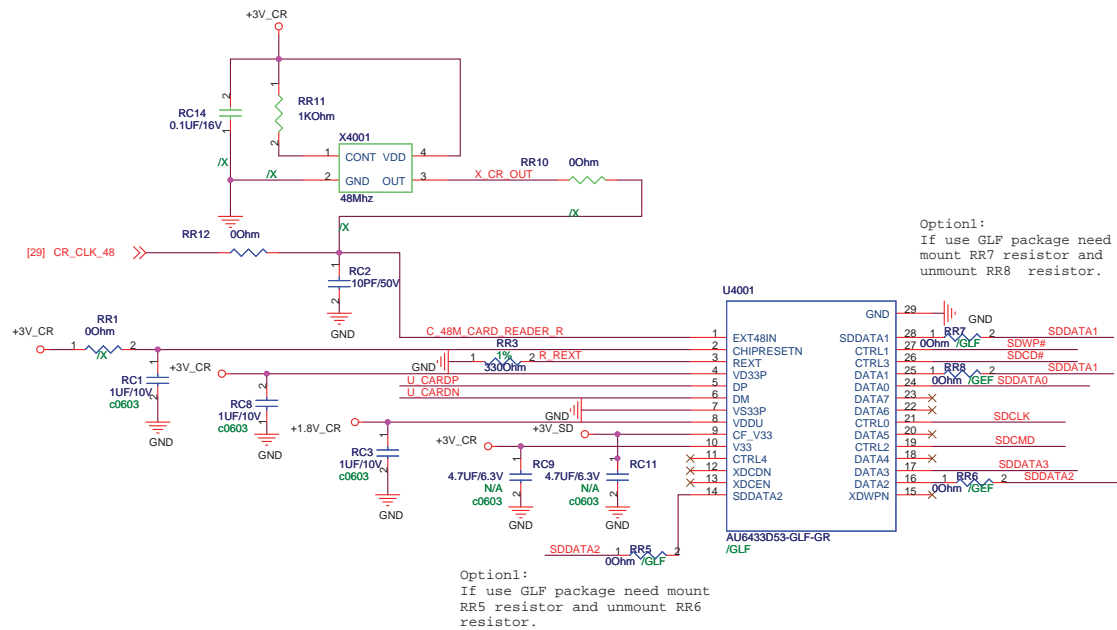
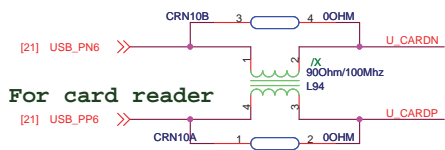
Reserve Pull high



Connect with SB OR EC



<Variant Name>		ASUS Title : ACC	
ASUSTek Computer INC.		Engineer: N/A	
Size	Project Name	1215T	Rev 1.0
Custom			
Date: Tuesday, August 10, 2010	Sheet 38 of 70		



<Variant Name>

ASUS Title : CB_AU-6433

ASUSTeK COMPUTER INC Engineer: N/A

Size	Project Name	Rev
11.25cm x 17.75cm	ASUS CB_AU-6433	1.0

5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>		3.5G Module & External Antenna	
		Title :	
ASUSTek Computer INC.		Engineer: N/A	
Size	Project Name	Rev	
Custom	1215T	1.0	
Date: Tue Jul 10 2010	Sheet	41	of 80

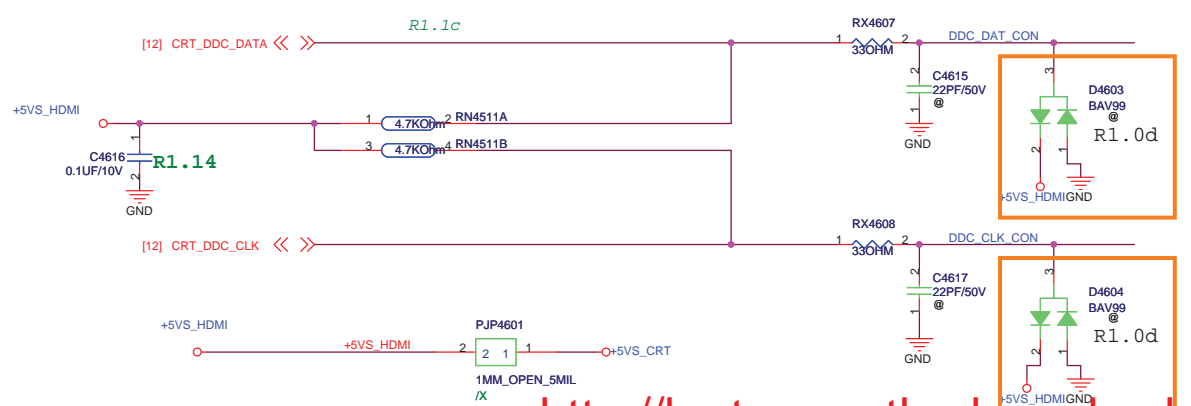
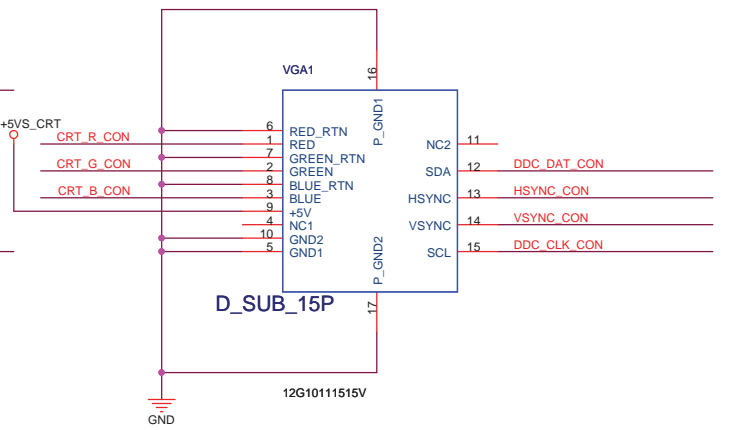
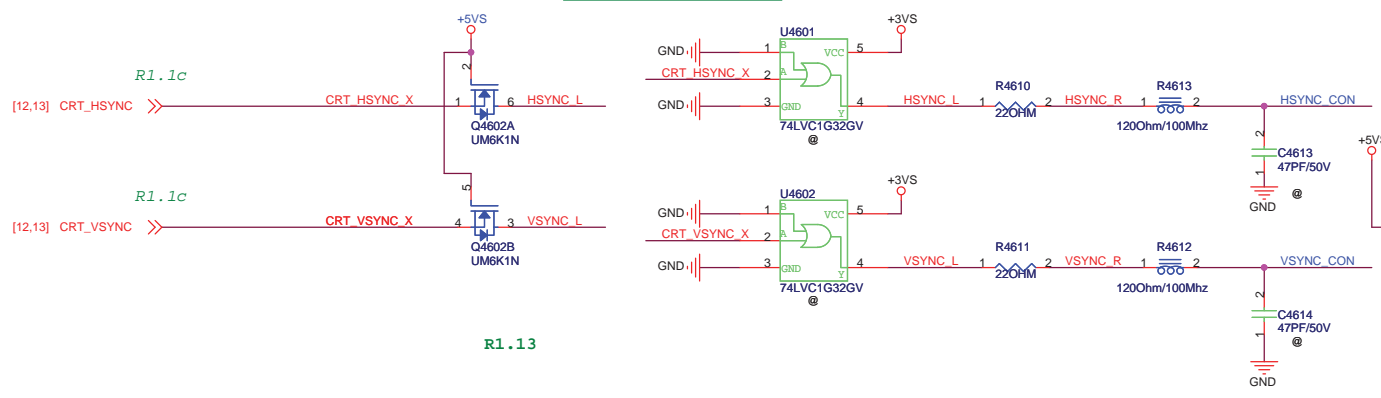
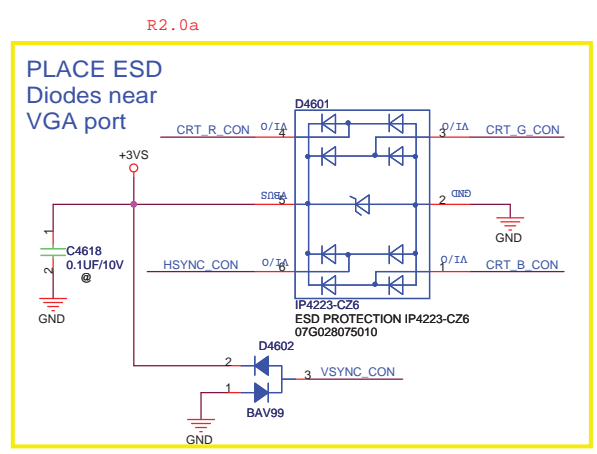
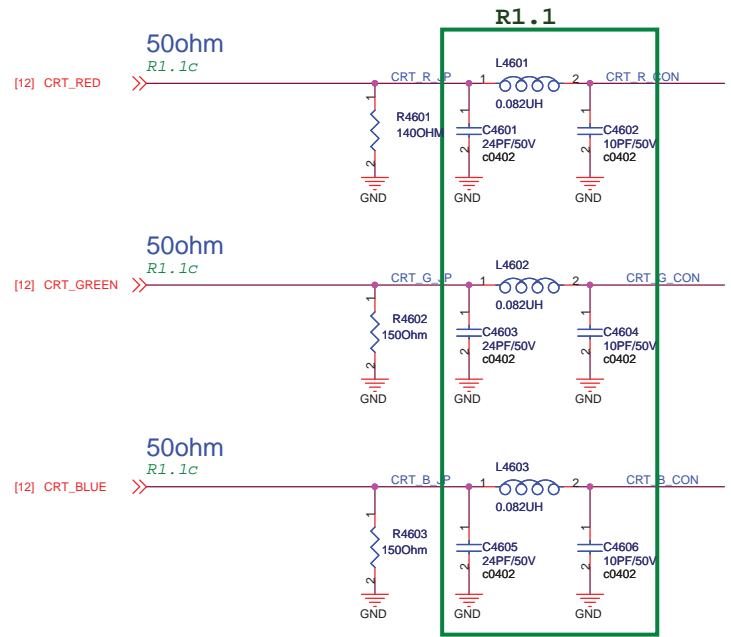
5

4

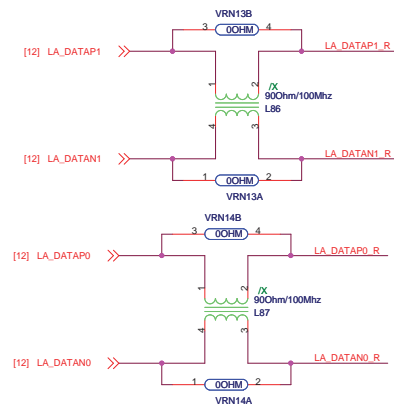
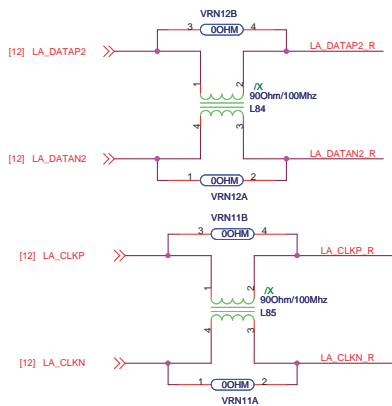
3

2

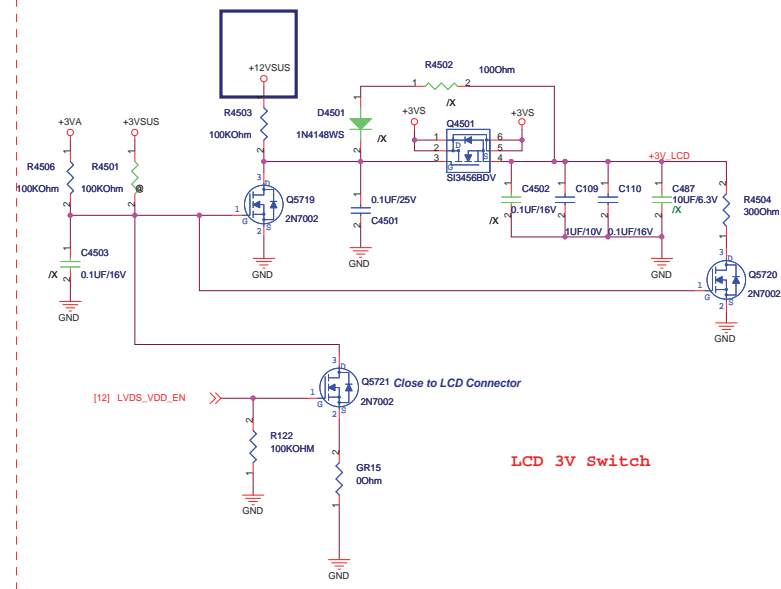
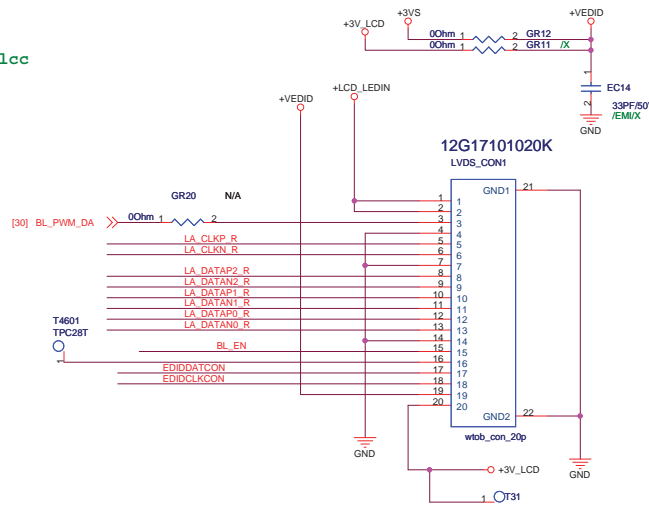
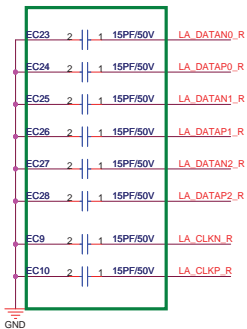
1



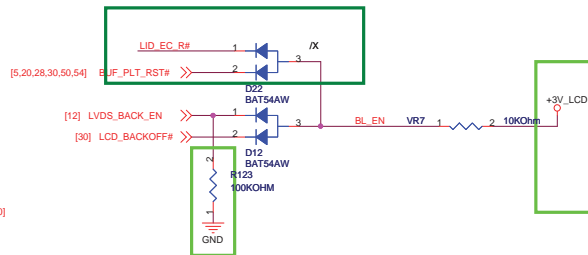
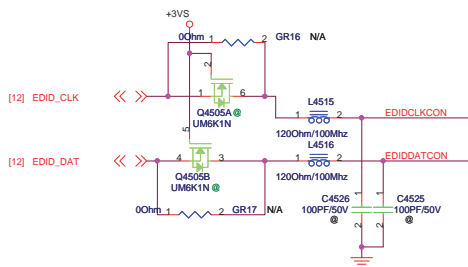
<http://laptop-motherboard-schematic.blogspot.com/>



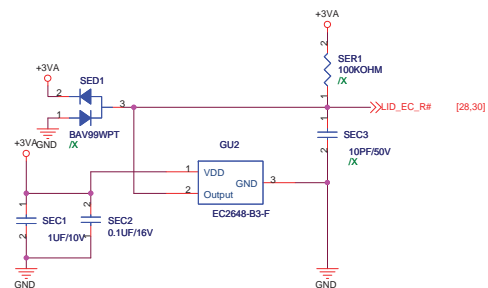
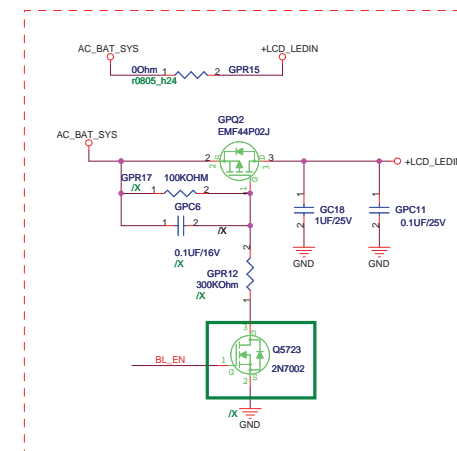
R1.1 FOR RF, mount this mlcc



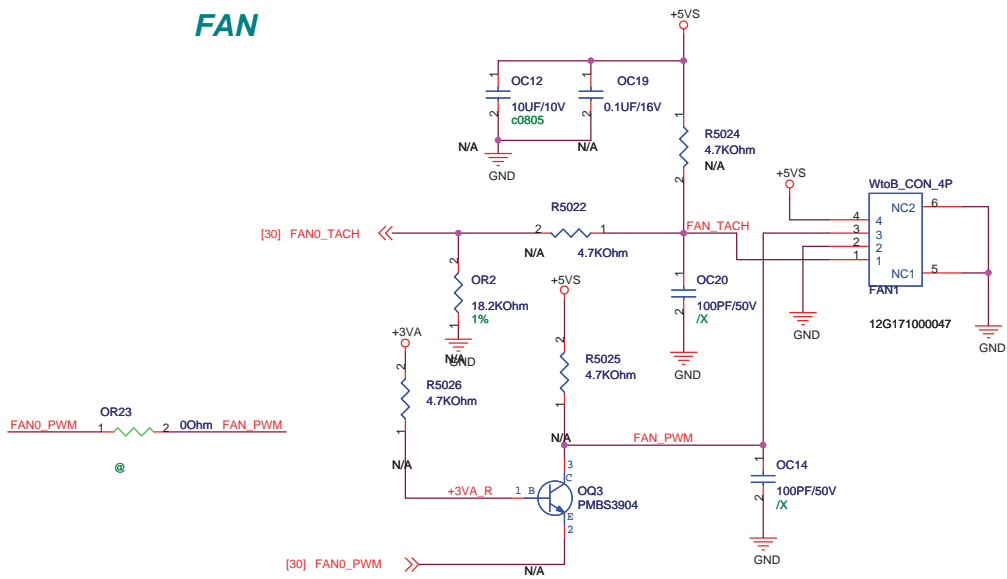
LCD 3V Switch



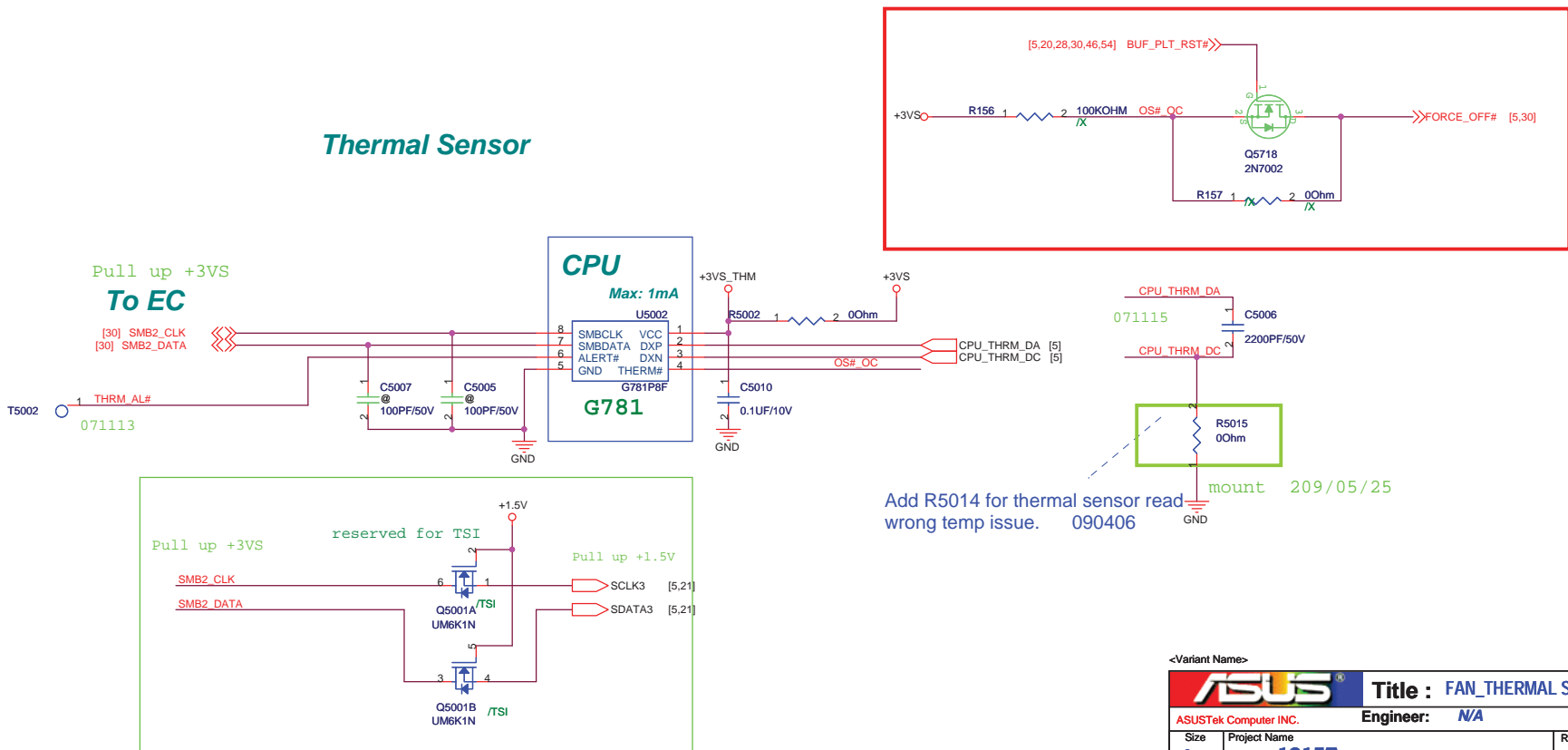
Backlight Enable Discharge



FAN




Thermal Sensor



ASUS		Title : FAN_THERMAL SENSOR	
ASUSTek Computer INC.		Engineer: N/A	
Size	Project Name	Rev	
Custom	1215T	1.0	
Date: Tuesday, August 10, 2010	Sheet	50	of 80

<http://laptop-motherboard-schematic.blogspot.com/>

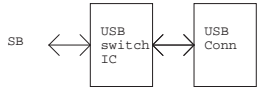
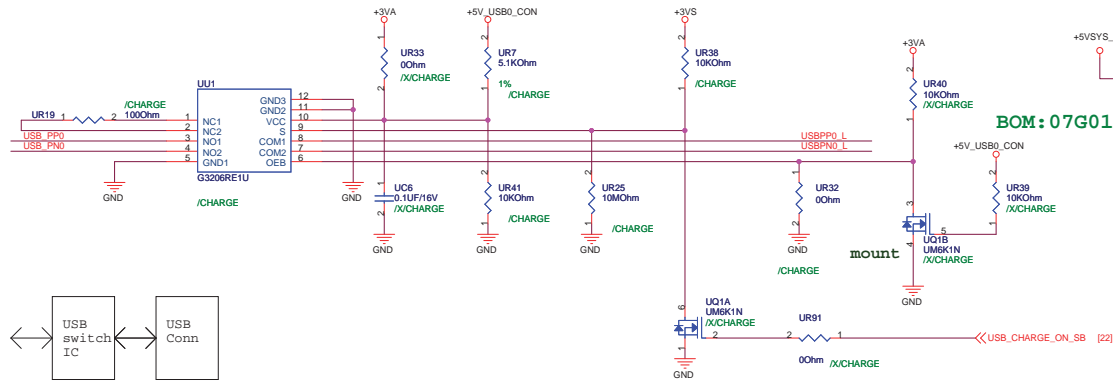
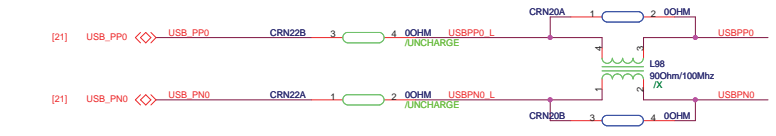
<Variant Names>

		Title : USB3.0 Fresco
ASUSTek Computer INC.		Engineer: N/A
Size	Project Name	Rev
C	1215T	1.0
Date: Tuesday, August 10, 2010		Sheet 51 of 80



		Title : USB 3.0_PORT
ASUSTeK COMPUTER INC. NB4		Engineer: NA
Size	Project Name	Rev
Custom	1215P	1.0
Date: 10/24/11	By: J. Liu	11/20/11
2	Sheet 1	52 of 80

USB2.0 with charge Connector(Optional)

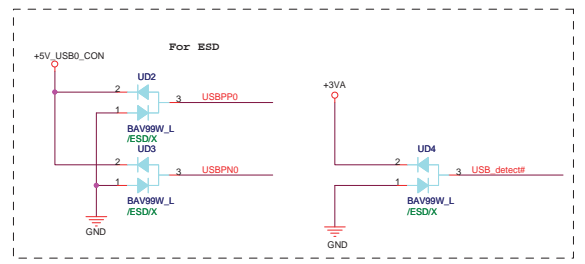


Function Table

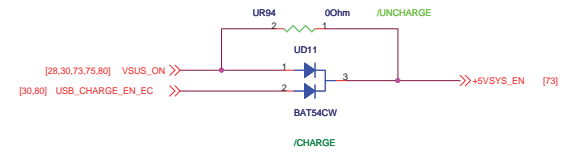
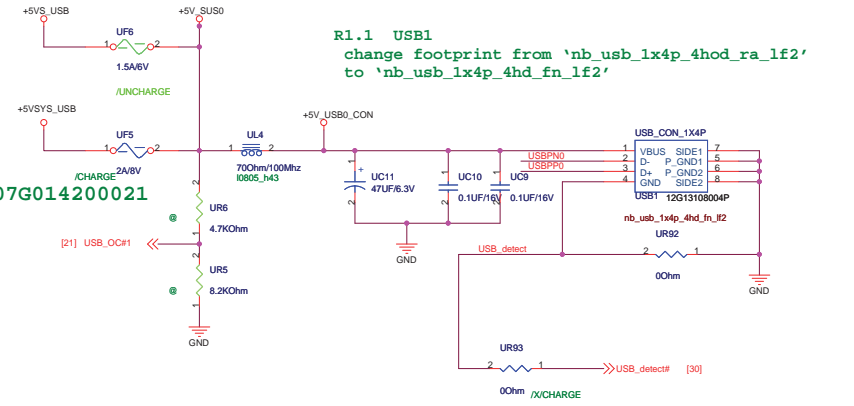
S	OEB	FUNCTION
X	H	Switch Disconnected
L	L	NC connected to Com
H	L	NO connected to Com

mount UQ1 in the BOM

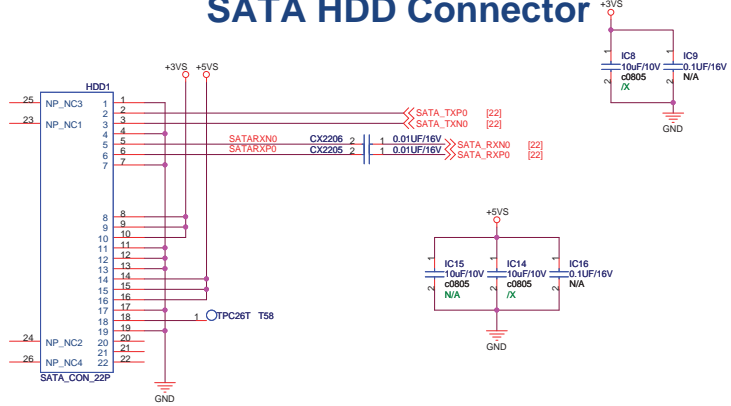
BOM: 07G014200021



R1.1 USB1
change footprint from 'nb_usb_1x4p_4hod_ra_1f2'
to 'nb_usb_1x4p_4hd_fn_1f2'

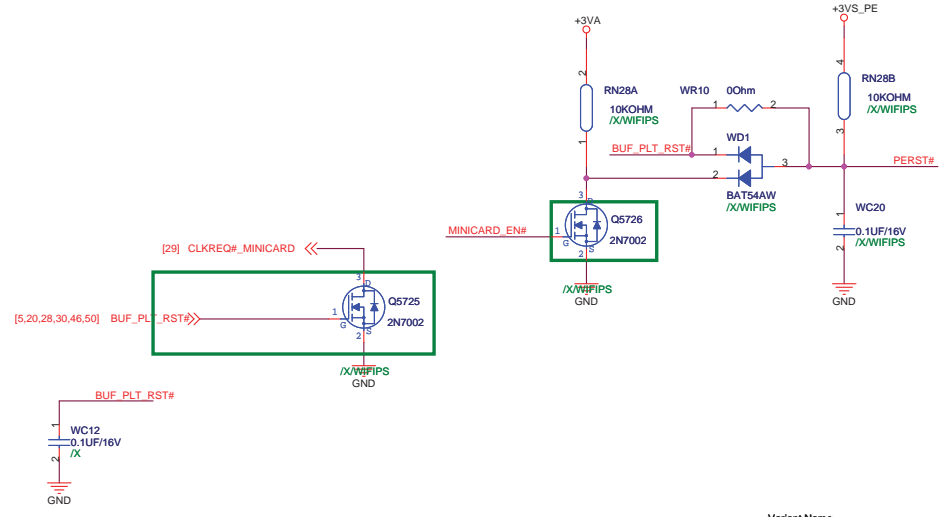
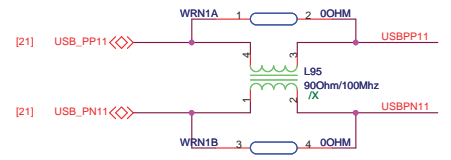
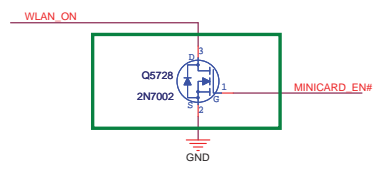
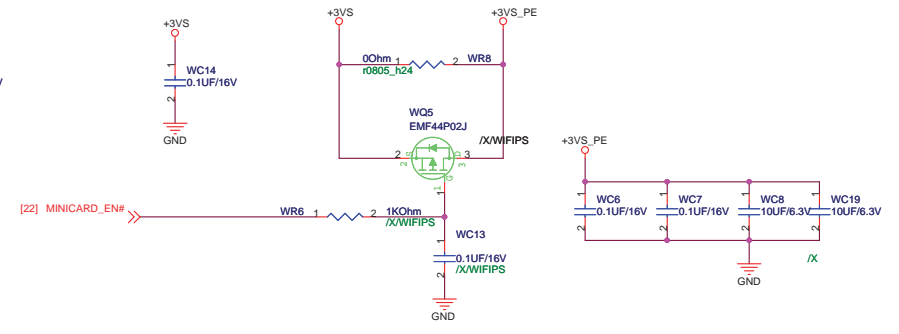
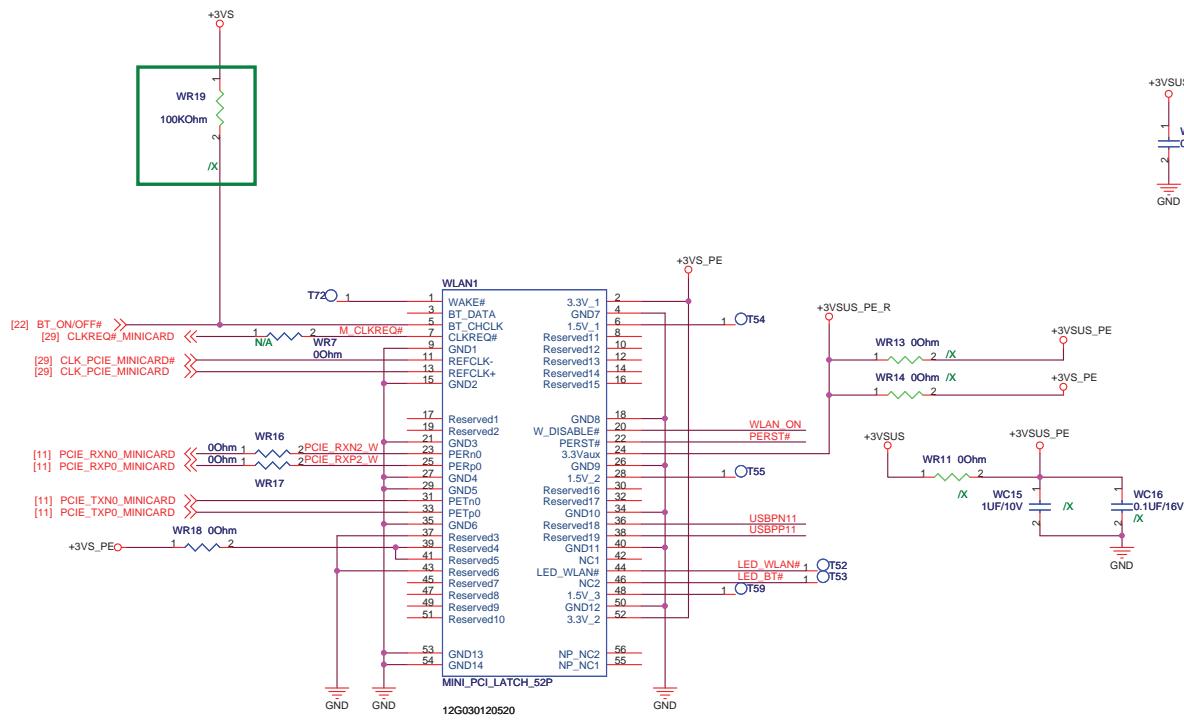


SATA HDD Connector

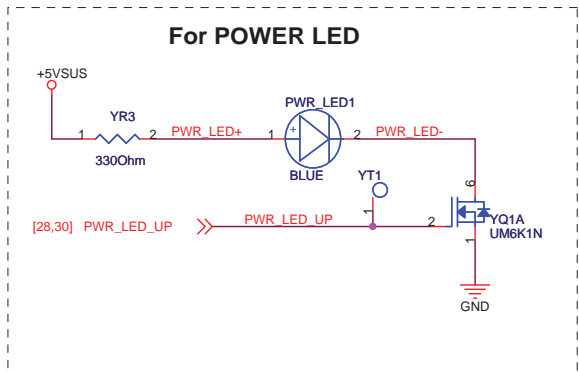


USB2.0 Connector

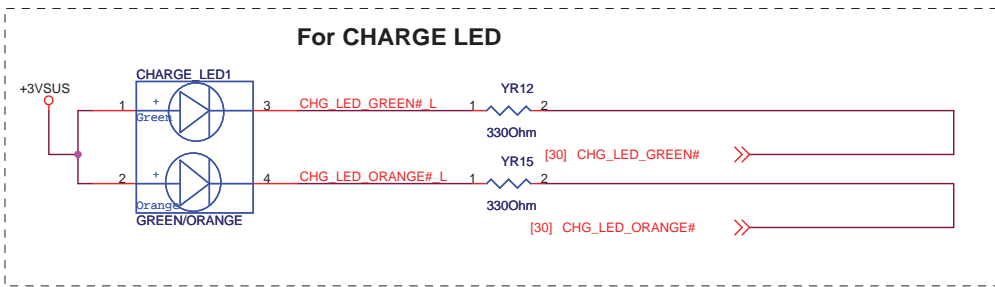
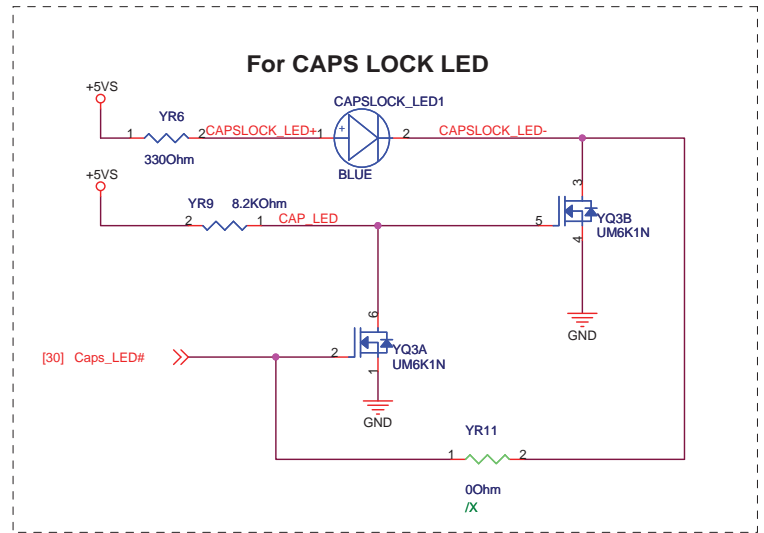
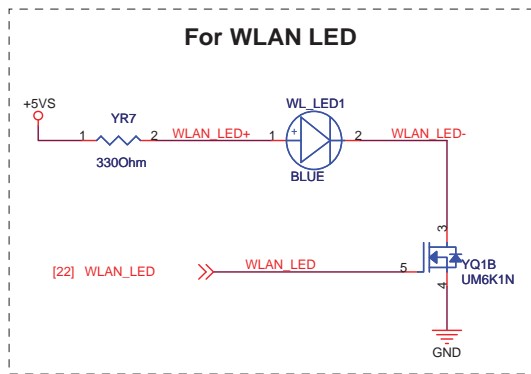
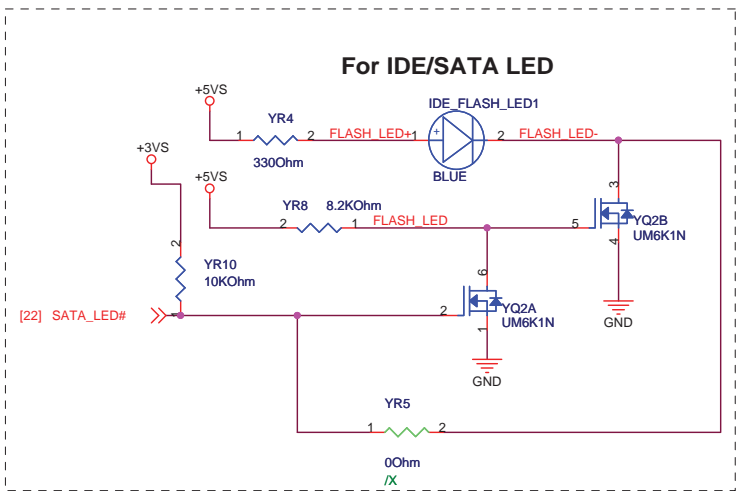




<Variant Name>		ASUS Title : Mini WiFi	
ASUSTek Computer INC.		Engineer: N/A	
Size Custom	Project Name 1215T	Rev 1.0	
Date: Tuesday, August 10, 2010		Sheet 54 of 80	

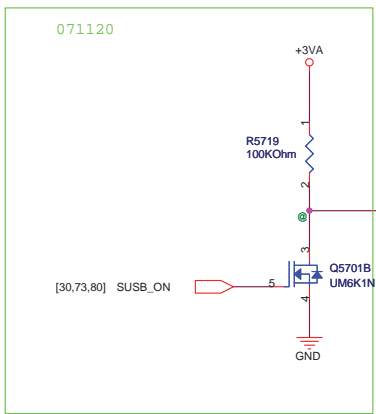
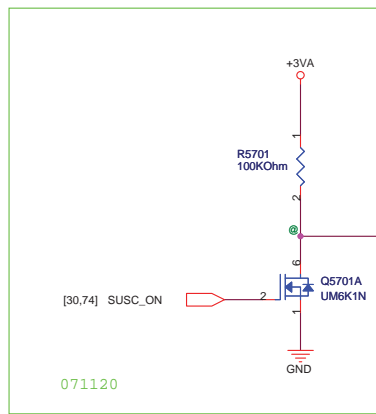


Mode	Adapater Mode	Battery Mode
Battery power is between 100%~40%	Orange ON	Green ON
Battery power is between 40%~10%	Orange Blinking Slowly	Green Blinking Slowly
Battery power is less than 10%	Orange Blinking Quickly	OFF
S3/S5 Mode	Scenario the same as above	

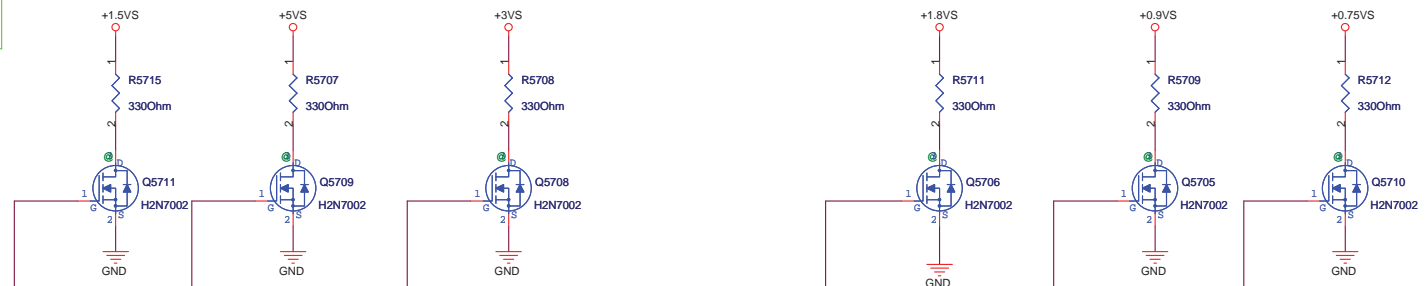


<Variant Name>

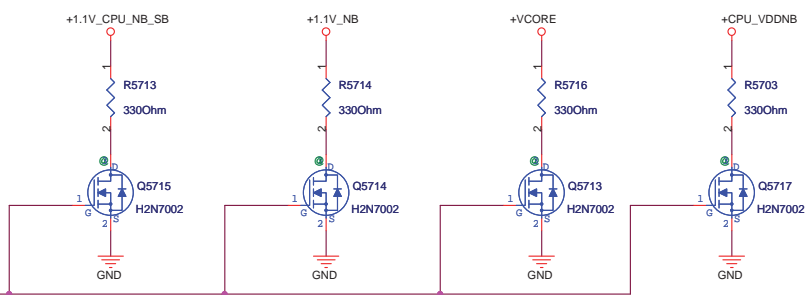
ASUS		Title : LED/PWR SWICH
ASUSTeK COMPUTER INC		Engineer: NA
Size	Project Name	Rev
B	1215T	1.0
Date: Tuesday, August 10, 2010		Sheet 56 of 80



Change net name

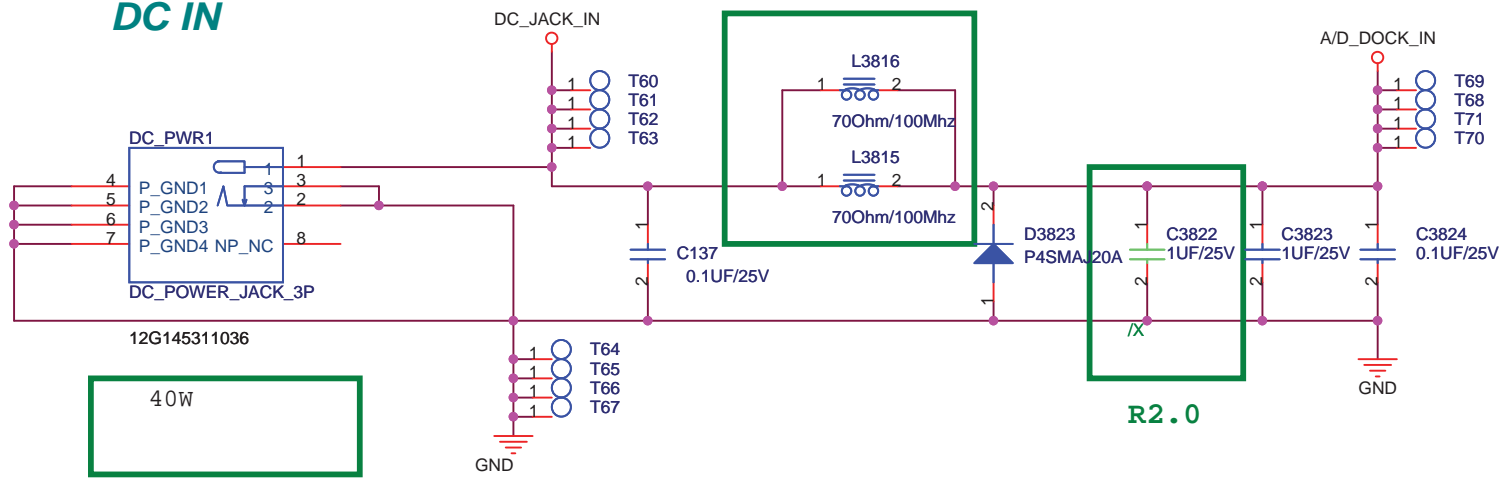


Change all MOS with ESD part



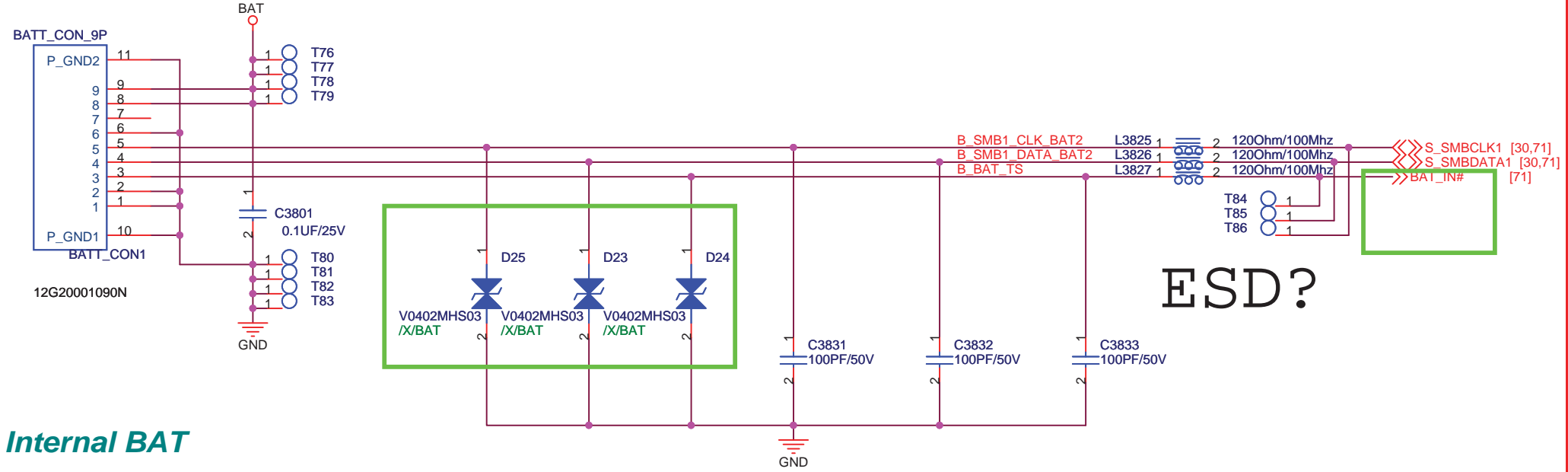
<Variant Name>		ASUS		Title : DISCHARGE CKT	
ASUSTeK COMPUTER INC		Engineer: N/A			
Size	Project Name	Rev			
Custom	1215T	1.0			
Date: Tuesday, August 10, 2010	Sheet	57	of	80	

DC IN



R2.0

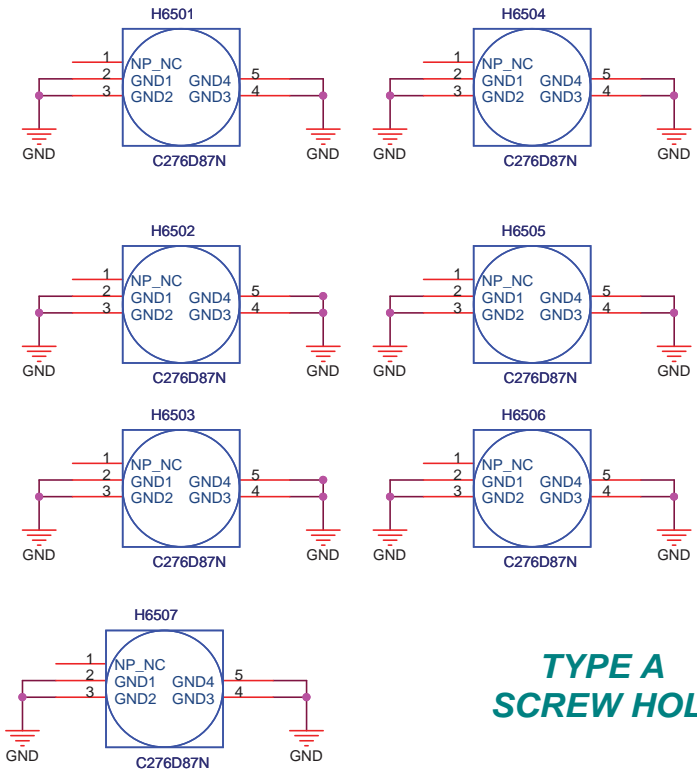
BATT_CON_9P



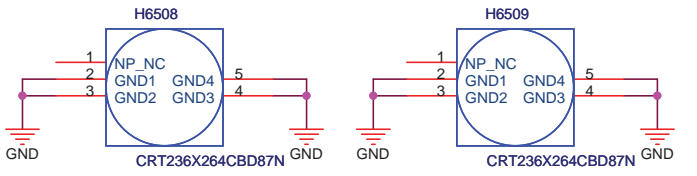
Internal BAT

<Variant Name>

ASUS		Title : PWR Jack	
ASUSTek Computer INC.		Engineer: N/A	
Size	Project Name	Rev	
A4	1215T	1.0	
Date: Tuesday, August 10, 2010	Sheet	60	of 80



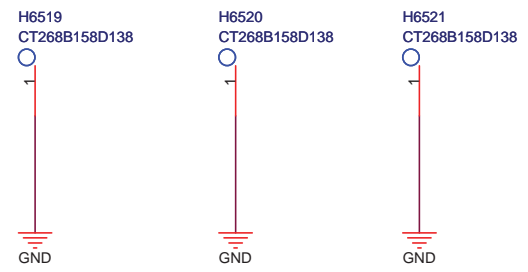
**TYPE A
SCREW HOLE**



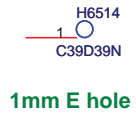
**TYPE B
SCREW HOLE**



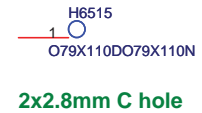
**TYPE C
SCREW HOLE**



CPU Bracket Hole



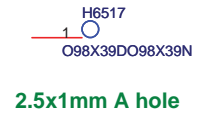
1mm E hole



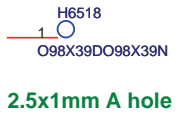
2x2.8mm C hole



2mm B hole

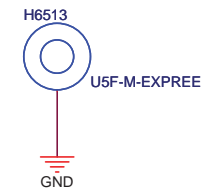
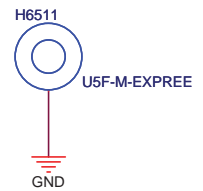


2.5x1mm A hole



2.5x1mm A hole

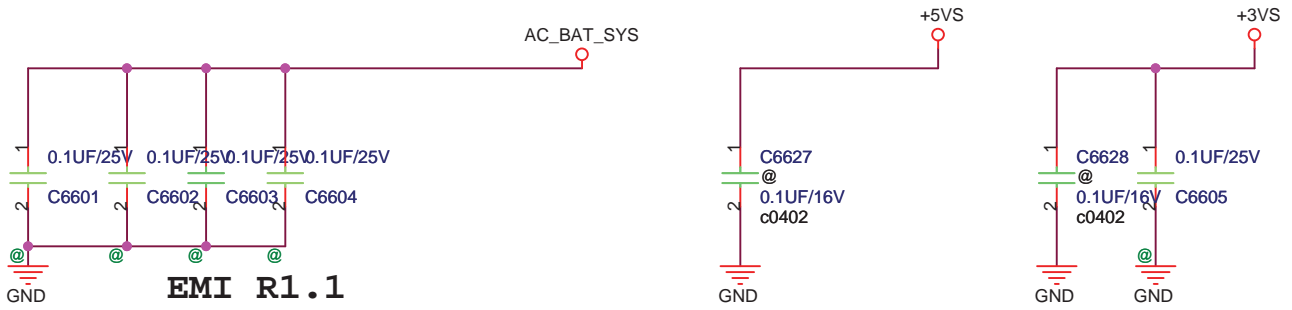
HOLE



NUT

<Variant Name>

		Title : Screw Hole	
ASUSTek Computer INC.		Engineer: N/A	
Size Custom	Project Name 1215T	Rev 1.0	
Date: Tuesday, August 10, 2010		Sheet	65 of 80



EMI R1.1



<Variant Name>


		Title : EMI	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	1215T	1.0	
Date: Tuesday, August 10, 2010		Sheet	66 of 80

ADD
0518:
add EMI Cap;
add R4806/R4807/Q4804
0520:
addT4601/PR167

DELETE
0520:
DEL PC85 PR107 PR12 PR87


MODIFY
0517:
switch TP button PIN1 to PIN3;PIN2 to PIN4

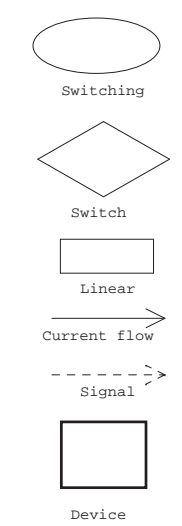
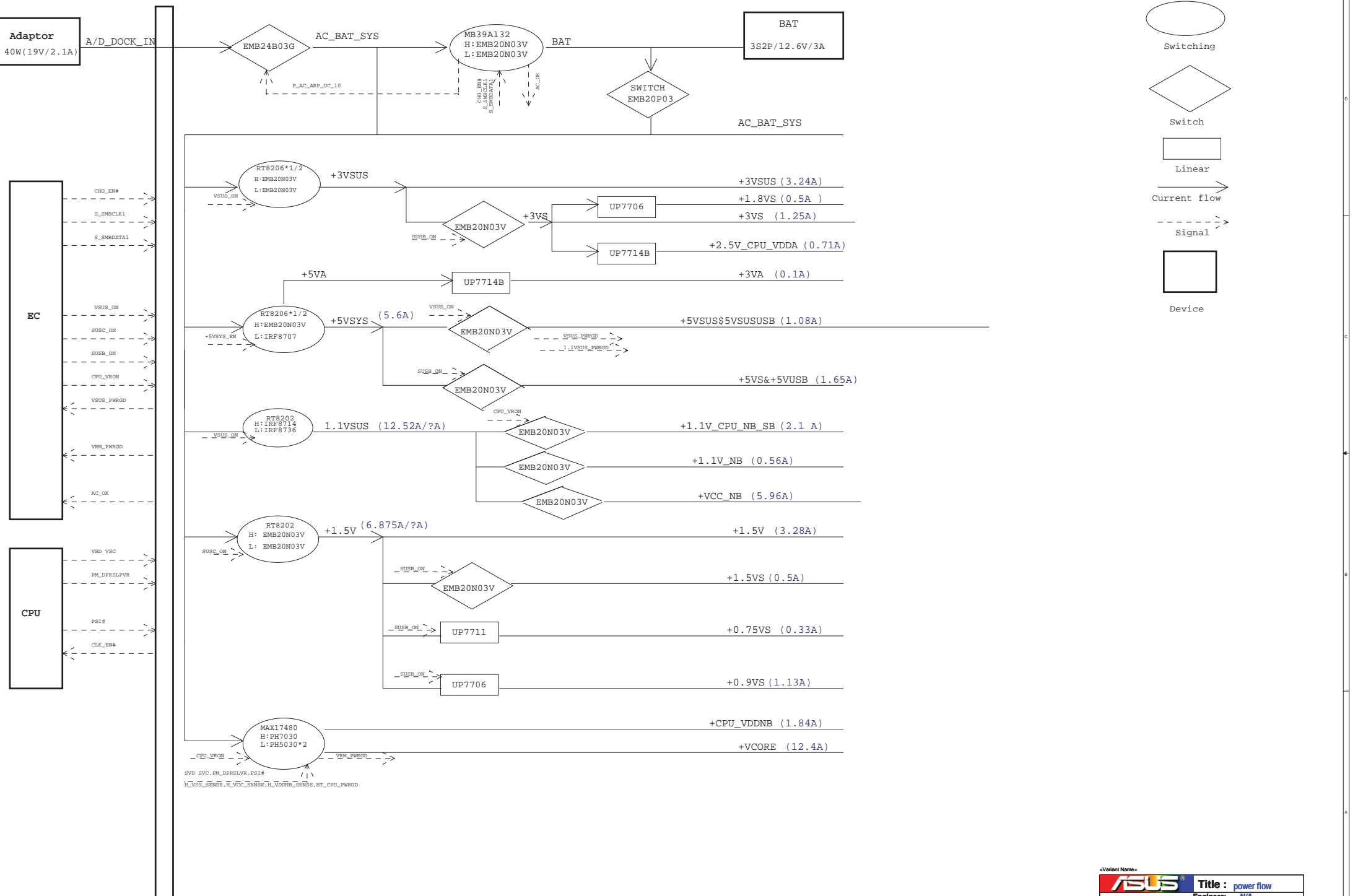
<Variant Name>

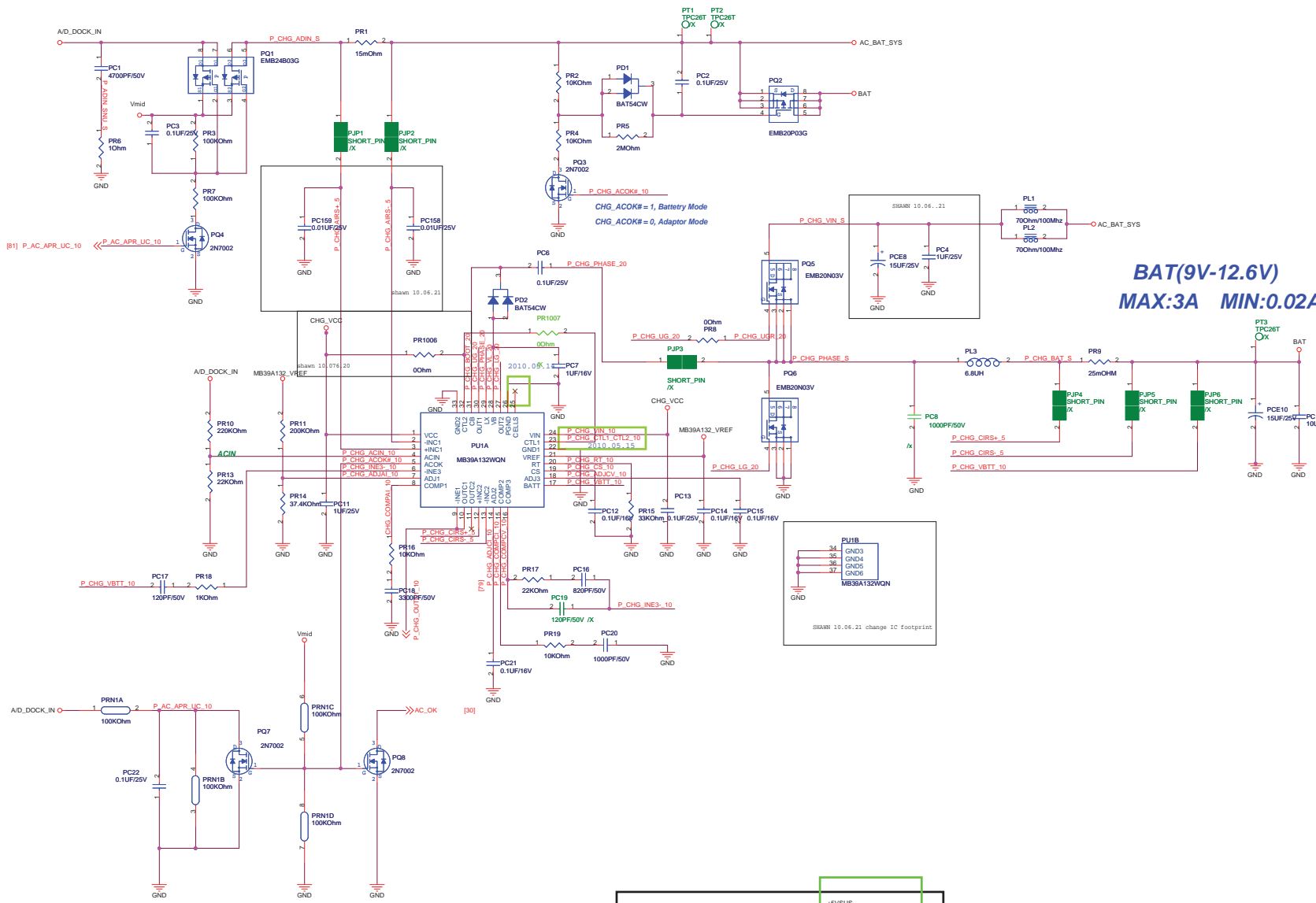
		Title : History	
ASUSTek Computer INC.		Engineer: N/A	
Size B	Project Name 1215T	Rev 1.0	
Date: Tuesday, August 10, 2010		Sheet 68	of 80

<http://laptop-motherboard-schematic.blogspot.com/>

<Variant Name>

		Title : Small borad
ASUSTek Computer INC.		Engineer: N/A
Size C	Project Name 1215T	Rev 1.0
Date: Tuesday, August 10, 2010	Sheet 69	of 80





Power Info

- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.9 \cdot V_{in}) = 2.1A$
- Ripple Current:**
 $I_{ripple} = 1.45A$
 $I_{spec} = 2.5A$
- Frequency:**
 $RT = 33KOHM$
 $F_{osc} = 17000 / RT(Kohm) = 515KHz$

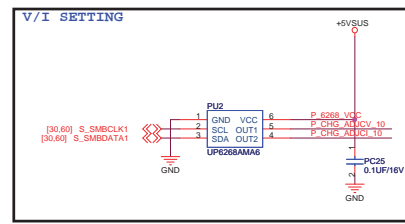
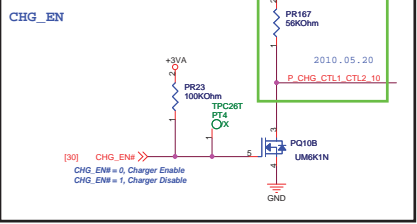
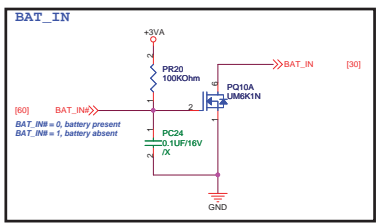
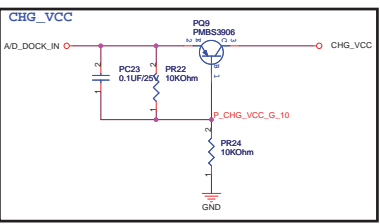
Battery Charging Current :
 $I_{chg} = (V_{adj} - 2.075) / (25 \cdot R_s)$
Input Adaptor Max. Current Limit :
 $I_{limit_current} = (V_{adj} - 1.075) / (25 \cdot R_s) = 1.90A$

ACIN Threshold = 1.25V
 Adaptor > 13.75V, System Powered by Adaptor
 Adaptor < 13.75V, System Powered by Battery

Battery Charging Voltage :
 $V_{adj3} : VREF \implies V_{bat} = 4.2V / cell$
 $3.9V > V_{adj3} > 2.4V \implies V_{bat} = 4.35V / cell$
 $V_{adj3} : GND \implies V_{bat} = 4.0V / cell$
 $2.2V > V_{adj3} > 1.1V \implies V_{bat} = 2 \cdot V_{adj3} / cell$
Battery Cell Selection :
 CELLS: VREF \implies 4 Cells;
 CELLS: OPEN \implies 3 Cells;
 CELLS: GND \implies 2 Cells;

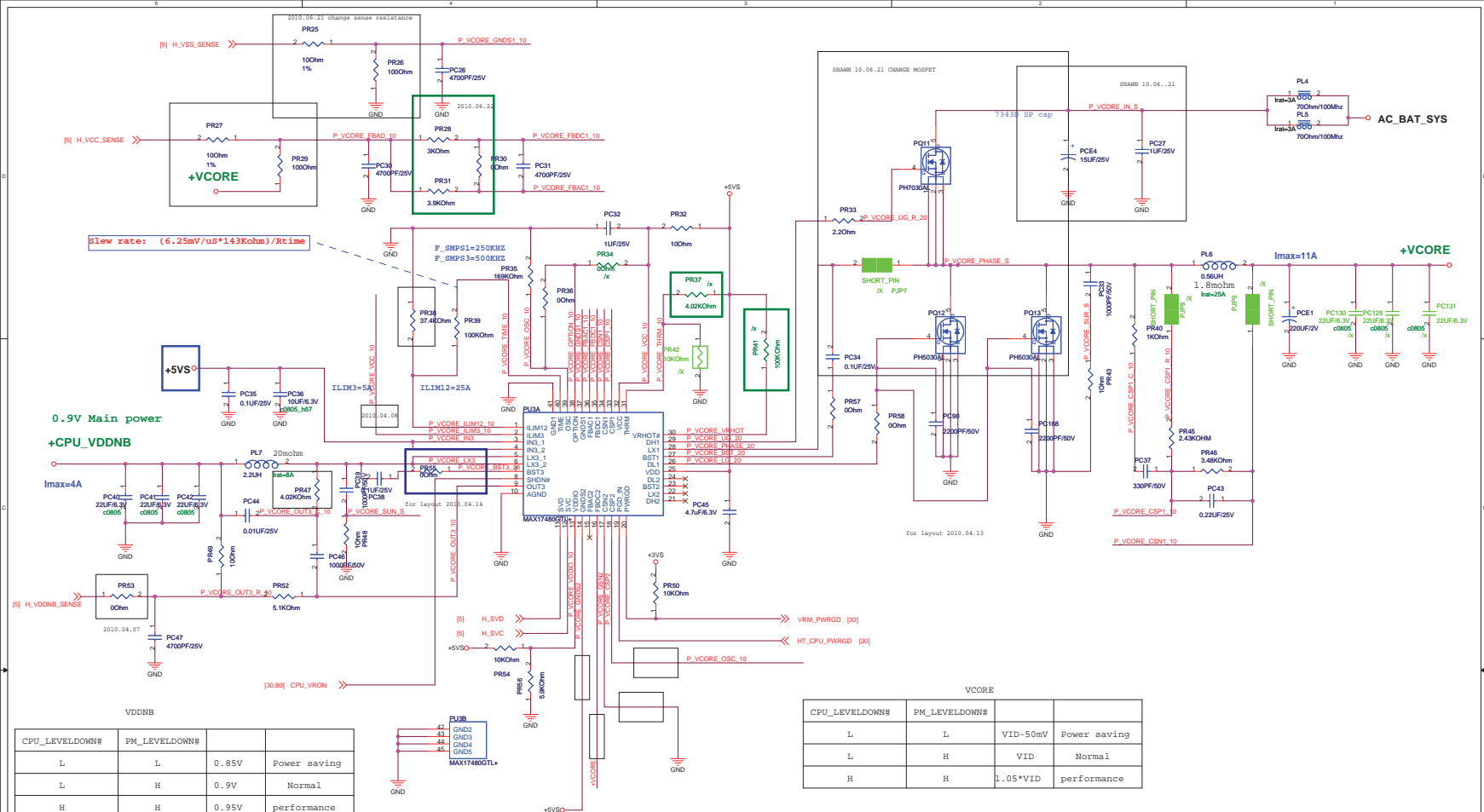
VREF = 5.0V
 $f_{osc}(KHz) = 17000 / RT (KOhm)$
 Soft start: $t_s(s) = 0.23 \cdot CS (\mu F)$

**BAT(9V-12.6V)
 MAX:3A MIN:0.02A**



<Variant Name>

ASUS		Title : Charger
ASUSTek Computer INC	Project Name	Engineer: N/A
Size: Custom	1215T	Rev: 1.1
Date: Tuesday, August 10, 2010	Sheet: 71	of 80



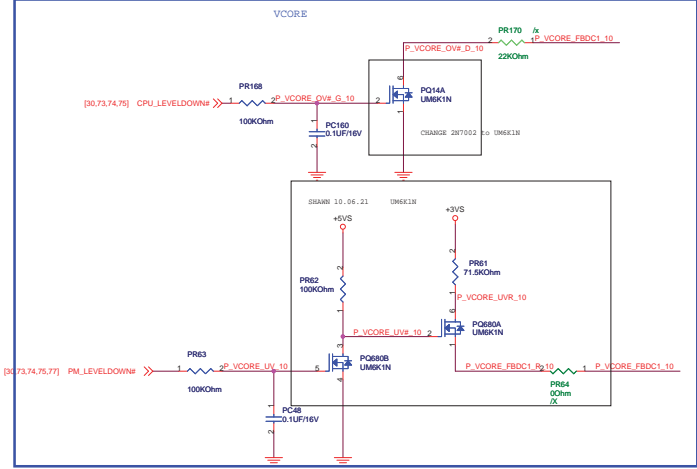
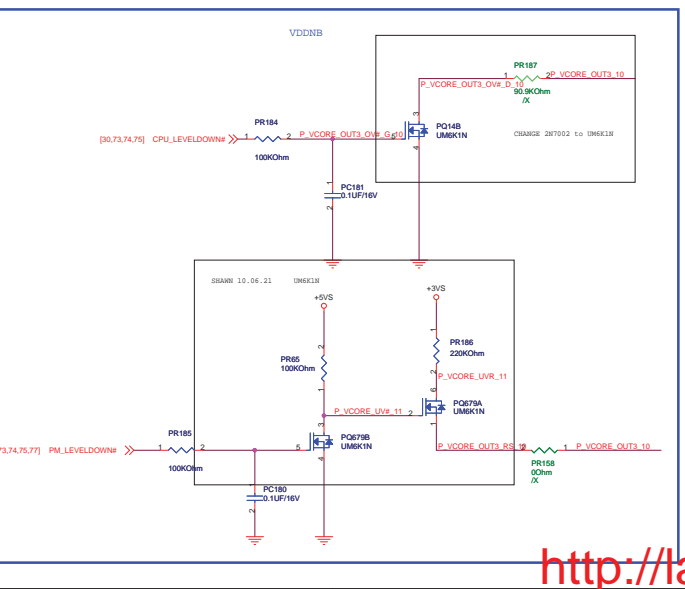
0.9V Main power
+CPU_VDDNB

VDDNB

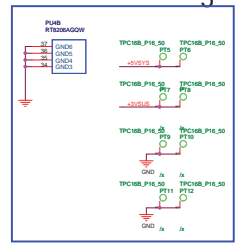
CPU_LEVELDOWN#	PM_LEVELDOWN#	VID	Power saving
L	L	0.85V	Power saving
L	H	0.9V	Normal
H	H	0.95V	performance

Vcore

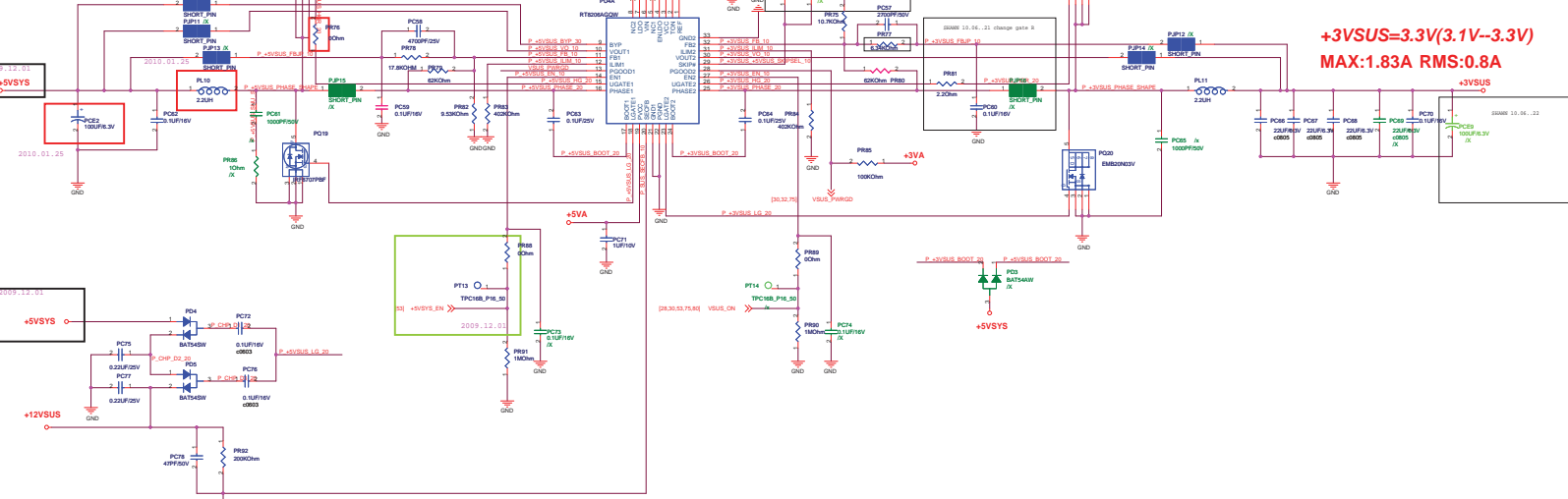
CPU_LEVELDOWN#	PM_LEVELDOWN#	VID	Power saving
L	L	VID-50mV	Power saving
L	H	VID	Normal
H	H	1.05*VID	performance



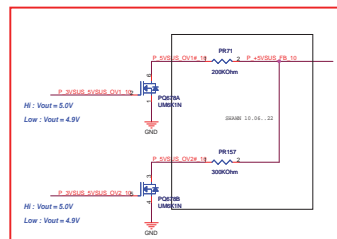
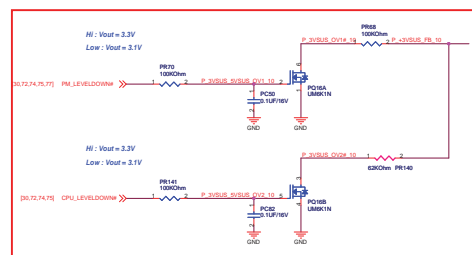
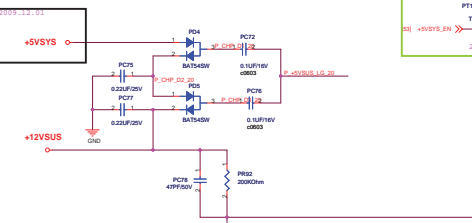
ASUS
ASUSTeK COMPUTER INC. NB
Title: Power Vcore
Engineer: Robin_chen
Project Name: 1215T
Rev: 0.1A
Date: Tuesday, August 10, 2010
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+5VSYS=5V(4.79V~5V)
MAX:6A RMS:1.3A

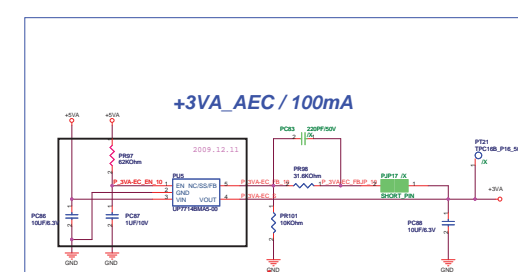


+3VSUS=3.3V(3.1V~3.3V)
MAX:1.83A RMS:0.8A



PM_LEVELDOWN#	CPU_LEVELDOWN#	Voltage	Status
L	L	3.15	Power Saving
H	L	3.30	Normal
H	H	3.45	Performance

PM_LEVELDOWN#	CPU_LEVELDOWN#	Voltage	Status
L	L	4.8	Power Saving
H	L	5.0	Normal
H	H	5.2	Performance



Power Info. +5VSUS

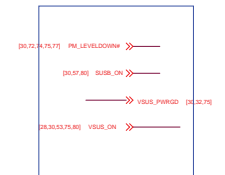
1. I/P Current:
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 2.082A$
2. Ripple Current:
 $I_{rip} = 1.482A$
 $I_{spec} = 2.5A$
 $O_1 = 1\text{ pcs}$
3. Frequency:
 $f_{osc} = 300KHz$
4. OCP:
 $I_{ocp} = 17A$

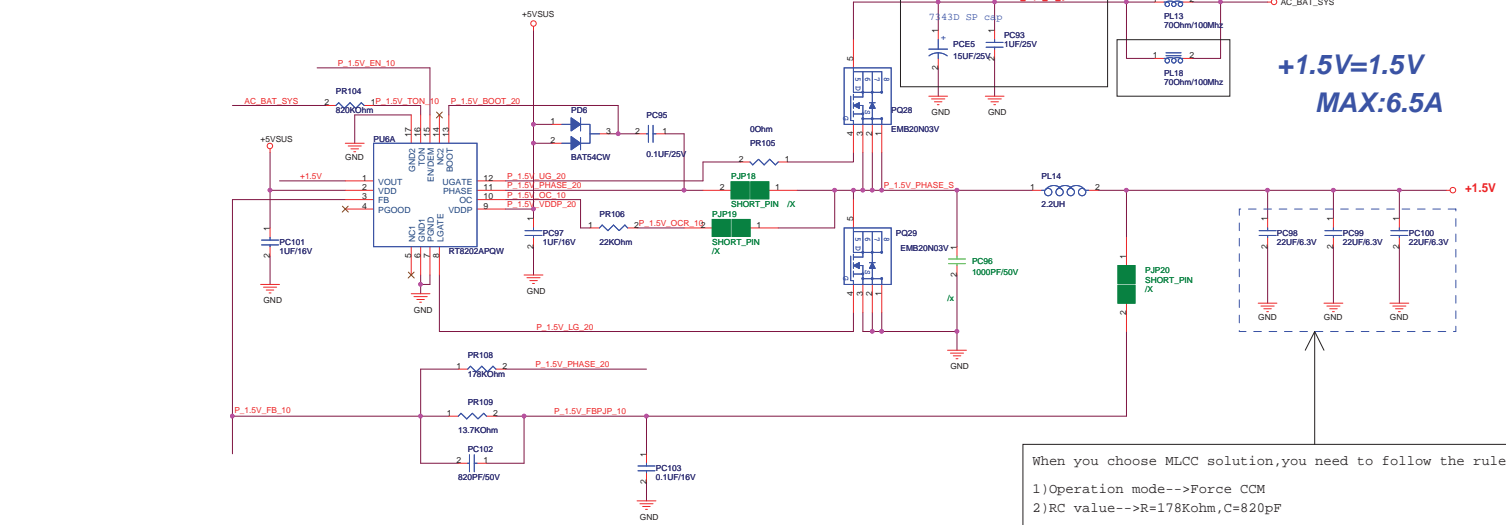
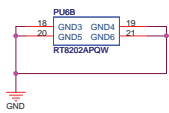
Power Info. +3VSUS

1. I/P Current:
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.832A$
2. Ripple Current:
 $I_{rip} = 1.92A$
 $I_{spec} = 2.5A$
 $O_1 = 1\text{ pcs}$
3. Frequency:
 $f_{osc} = 375KHz$
4. OCP:
 $I_{ocp} = 8.74A$

Power Info. +3VA

1. Dropout Voltage:
 $V_s = 210mV (I_o = 300mA)$
2. Current Limit:
 $I_{limit} = 480mA$
3. Pd:
 $R_{thjc} = 5\text{ C/W}$
 $P_d = 0.4W$





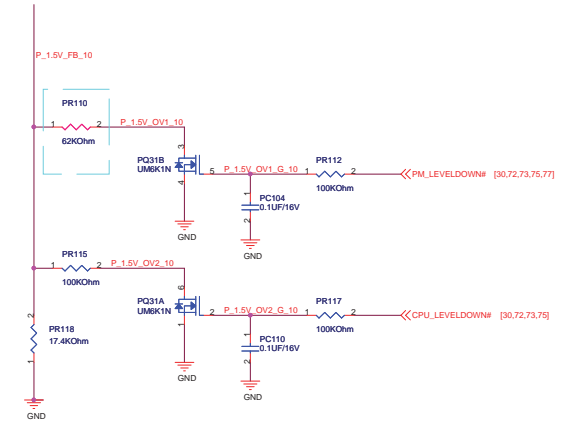
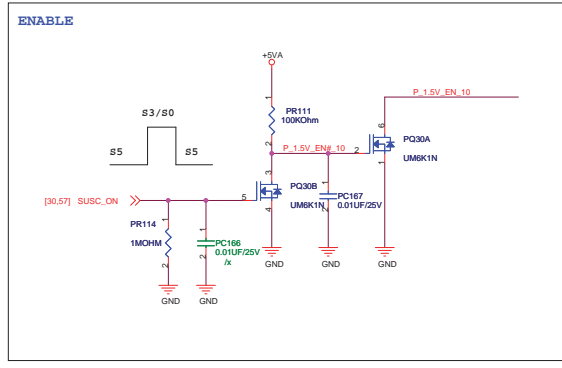
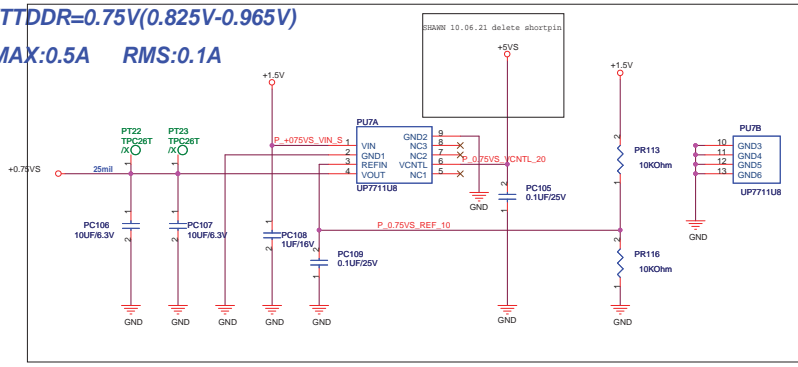
Power Info.

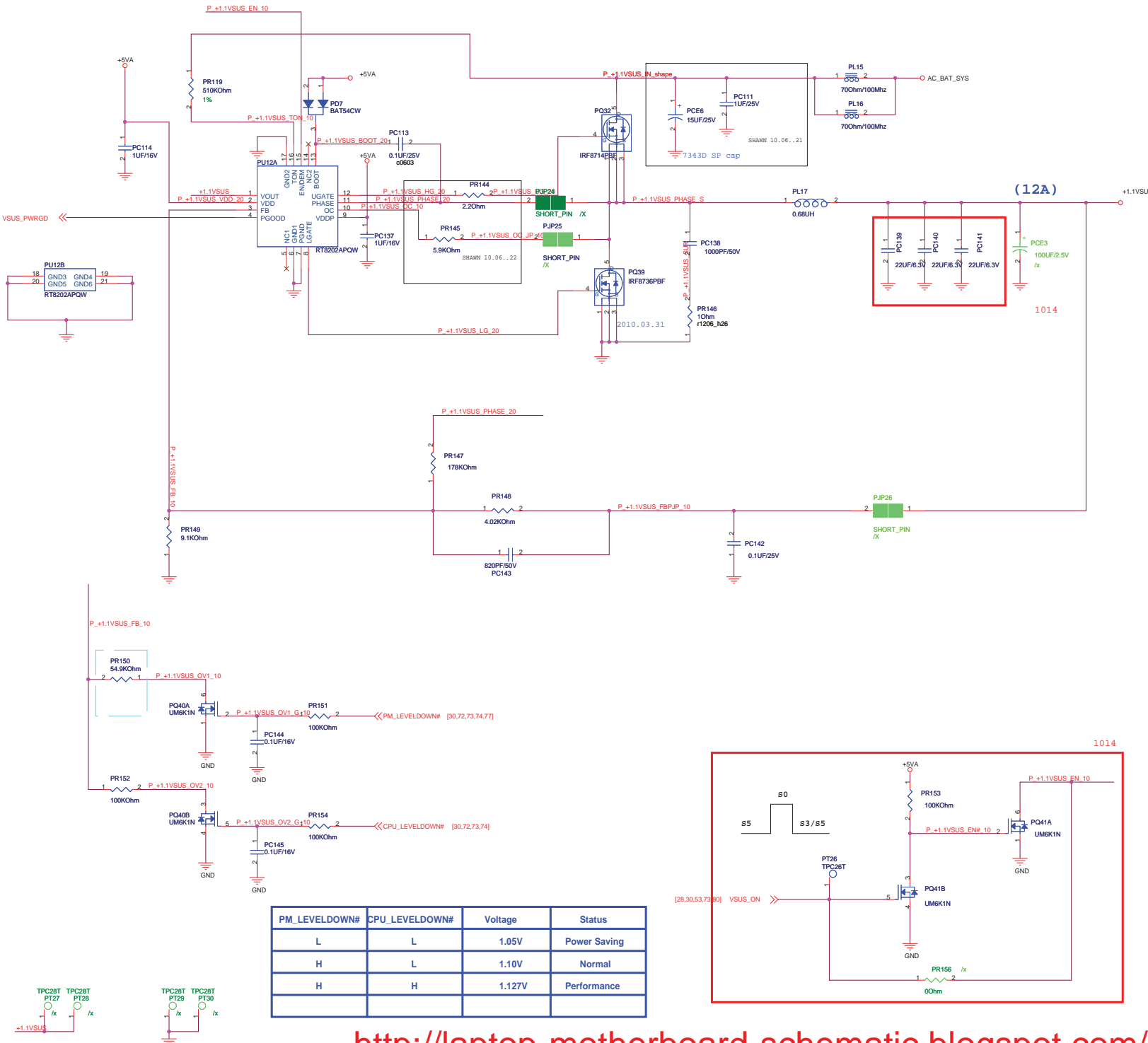
- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 0.825A$
- Ripple Current:**
 $I_{rip} = 1.32A$
 $I_{spec} = 2.5A$
- Dynamic:**
 $I_{peak} = 3.3A$
 $ESR = 18 \text{ mohm}$
 $V = 59.4mV$
- Frequency:**
 $F_{osc} = 300KHz$
- OCV:**
6.45A

When you choose MLCC solution, you need to follow the rule:
 1) Operation mode --> Force CCM
 2) RC value --> $R = 178Kohm, C = 820pF$

PM_LEVELDOWN#	CPU_LEVELDOWN#	Voltage	Status
L	L	1.4V	Power Saving
H	L	1.5V	Normal
H	H	1.6V	Performance

+VTTDDR=0.75V(0.825V-0.965V)
MAX:0.5A RMS:0.1A



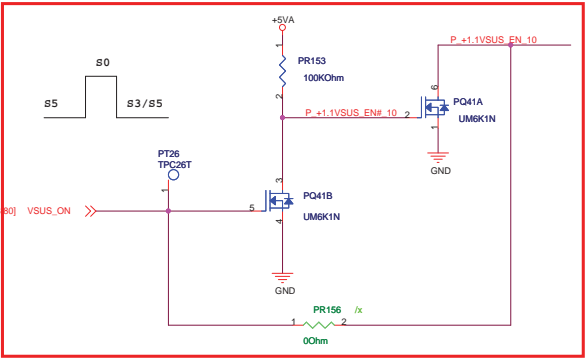


Power stage

- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.8 \cdot V_{in}) = 1.822A$
- Ripple Current:**
 $I_{ripple} = 3.73A$
- Ripple Voltage:**
 $I_{peak} = 10.933$
 $ESR = 18m\Omega$
 $V = 197mV$
- Inductor Spec:**
 $I_{sat} = 25A$
 $I_{dc} = 15.5A$
 $DCR = 5.5m\Omega$
- MOSFET Spec:**
H-side and L-side MOSFET:
 $R_{ds(on)} = 3020A$ ($T = 25$)
 $I_{peak} = 120A$ (Pause < 10us)

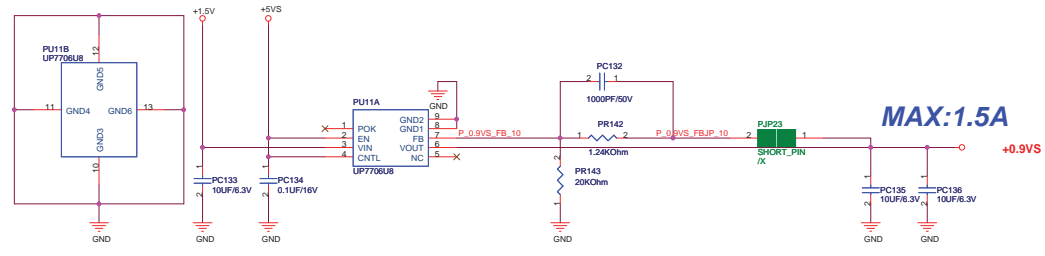
Controller

- Voltage & Current:**
 $+1.2VSUS = 1.2V \& 10.933A$
- Frequency:**
 $Frequency = 500KHZ$
- OCP:**
Set $PR146 = 5.9K\Omega$
 $I_{ocp} = R_{ocp} \cdot 20 / R_{ds(on)} = 20A$
- Soft start time:**
Soft-Star duration is 1.35ms
- Inrush Current:**
 $C_{total} = 66\mu F$
 $I_{inrush} = 0.088A$

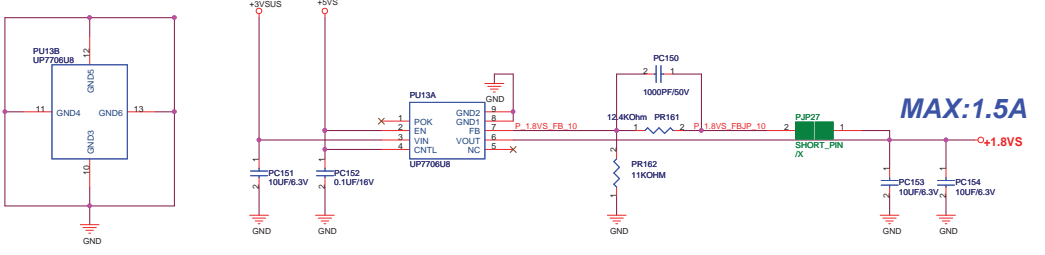


PM_LEVELDOWN#	CPU_LEVELDOWN#	Voltage	Status
L	L	1.05V	Power Saving
H	L	1.10V	Normal
H	H	1.127V	Performance

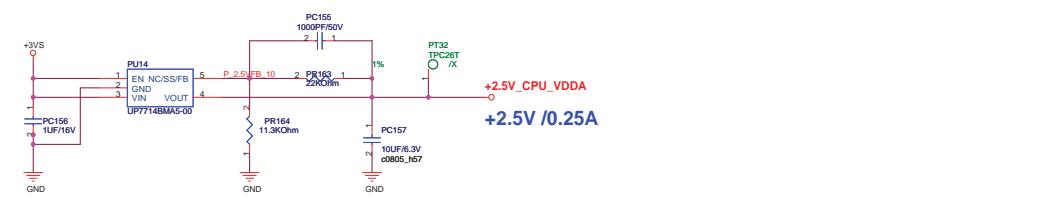
<http://laptop-motherboard-schematic.blogspot.com/>



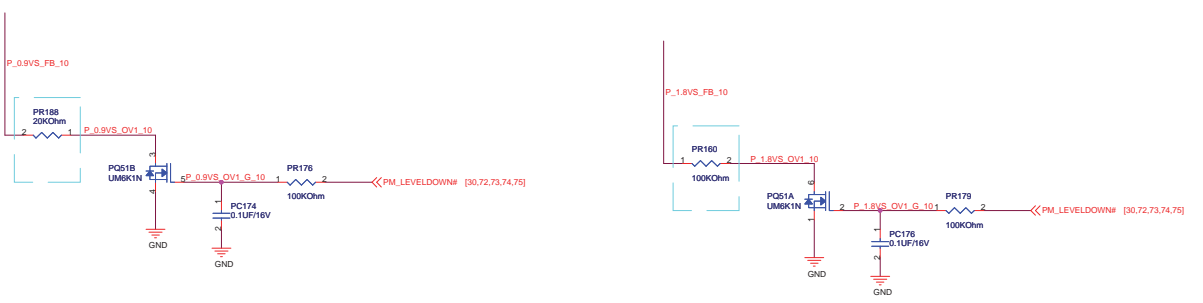
MAX:1.5A



MAX:1.5A



+2.5V /0.25A



- Dropout Voltage:
V = 300 mV (Io=2 A)
- Current Limit:
I limit= 2.8 A
- Continue Current:
I cont= 1A
- Pd:
R thjc =5 C/W
Pd =1.9W
- EN Voltage:
V rising = 1.4 V
V falling = 0.4 V
- Supply Voltage:
Vcc=5V
- Inrush current:
Tss = 4 ms
C total = 20 uF
I inrush= 7.5mA

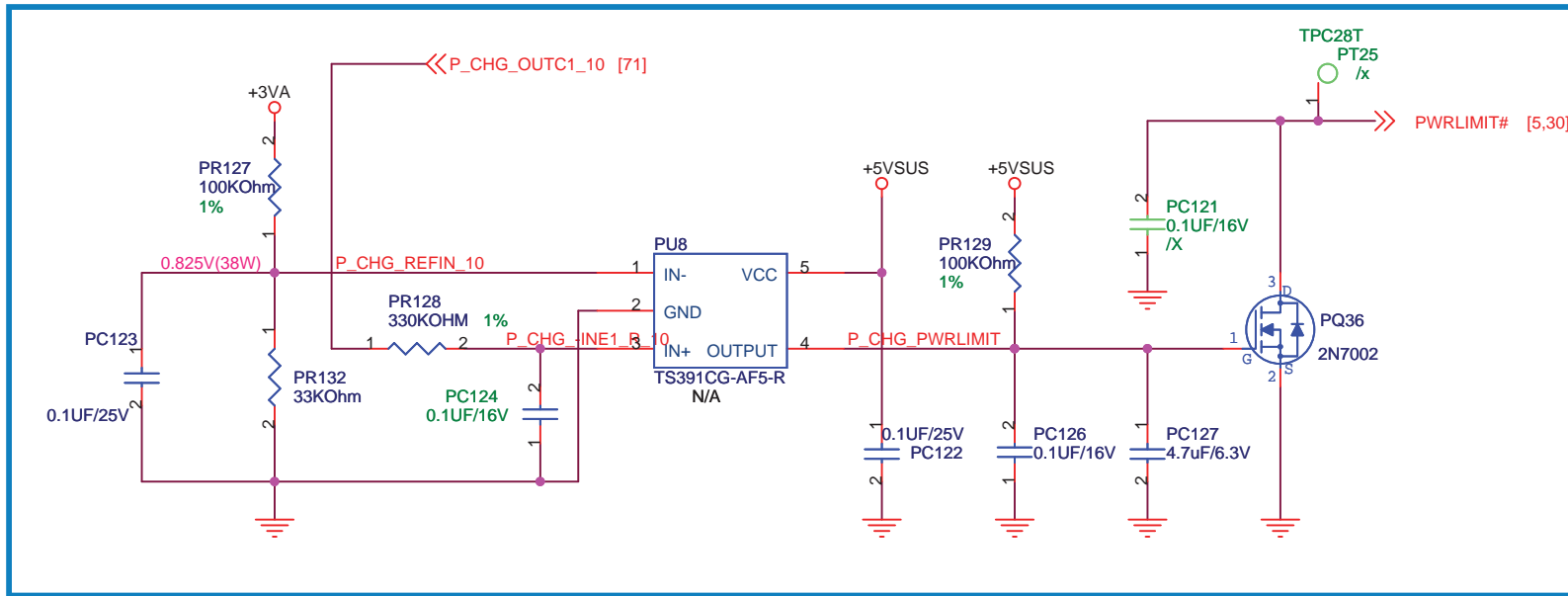
- 2.5V @ 0.25A
- Dropout Voltage:
V = 0.21V (Io =0.3A)
 - Current Limit:
I limit =320mA
 - Continue Current:
I cont = 300mA
 - Power Dissipation:
Rthjc = 250 /W
Pd = 0.1W
 - EN Voltage:
V rising = 2V
V falling = 0.8V
 - Supply Voltage:
Vcc =3V
 - Inrush current:
Tss = 400us
C total = 10uF
I inrush = 0.063A

+0.9VS

PM_LEVELDOWN#	CPU_LEVELDOWN#	Voltage	Status
L	L	0.85V	Power Saving
H	L	0.9V	Normal
H	H	0.95V	Performance

+1.8VS

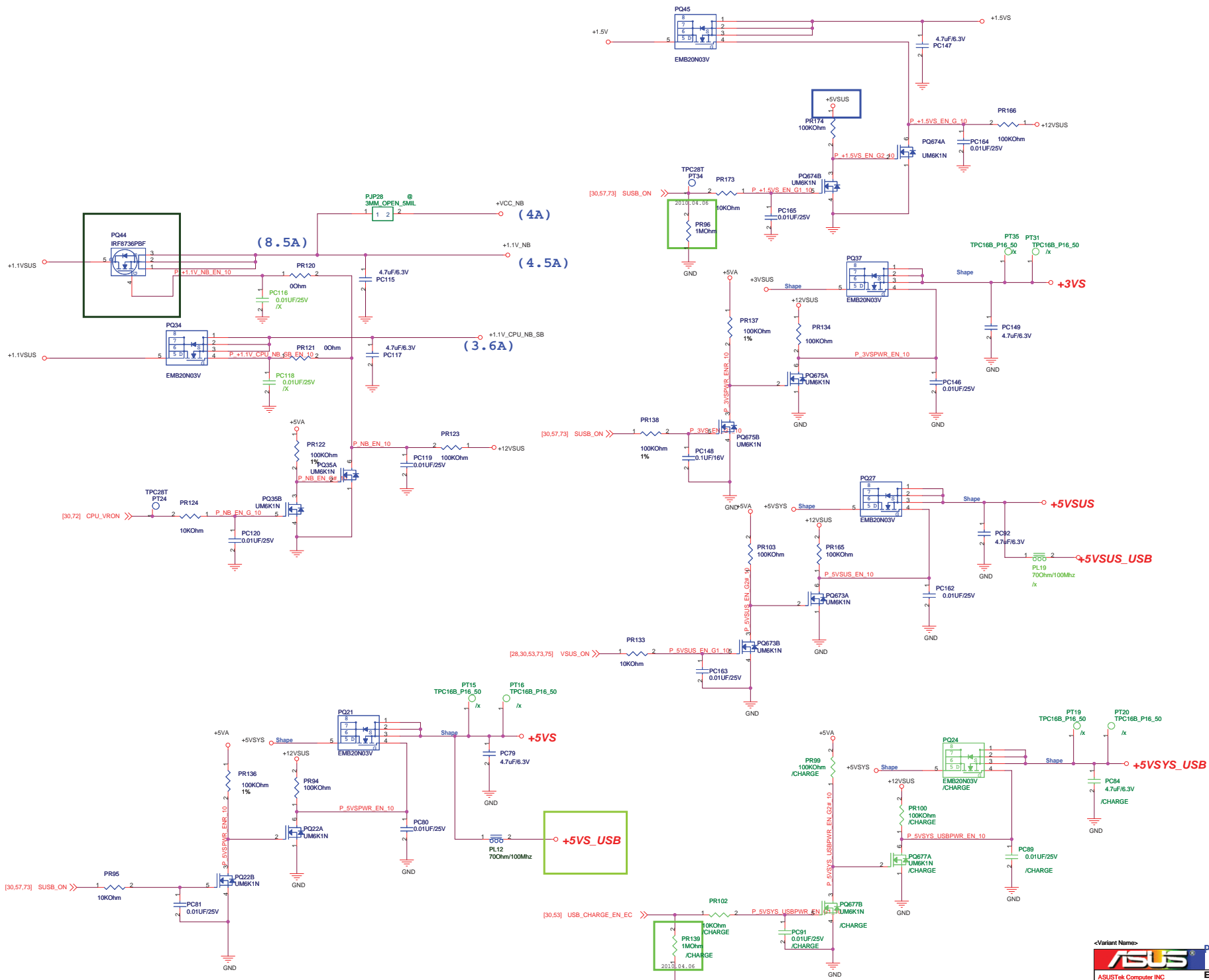
PM_LEVELDOWN#	CPU_LEVELDOWN#	Voltage	Status
L	L	1.7V	Power Saving
H	L	1.8V	Normal
H	H	1.9V	Performance



<Variant Name>

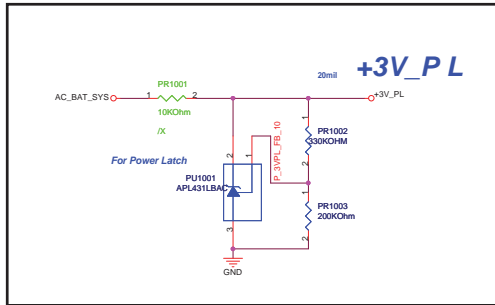
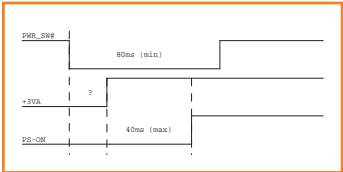
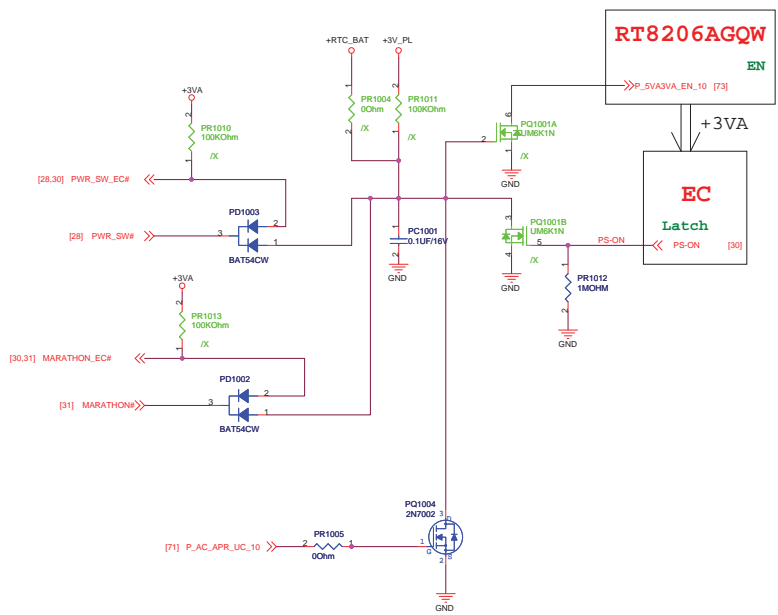
ASUS		Title : Power Lim
ASUSTek Computer INC		Engineer: N/A
Size	Project Name	Rev
A4	1215T	1.1
Date: Tuesday, August 10, 2010		Sheet 79 of 80

<http://laptop-motherboard-schematic.blogspot.com/>

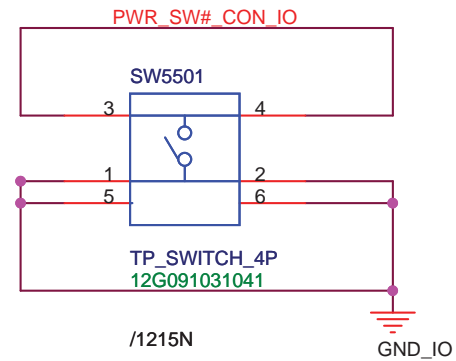
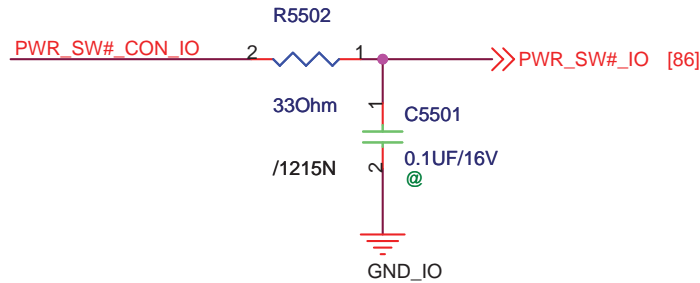


<http://laptop-motherboard-schematic.blogspot.com/>

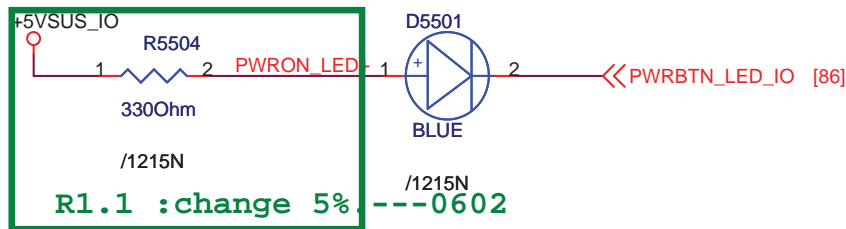
Variant Name:		Power_LOAD_SWITCH_OTHER	
ASUS		Title :	
ASUSTek Computer INC		Engineer: N/A	
Size	Project Name	Rev	
C	1215T	1.1	
Date: Tuesday, August 10, 2010	Sheet	80	of 81



PWR SW



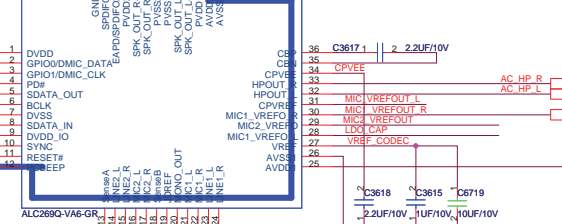
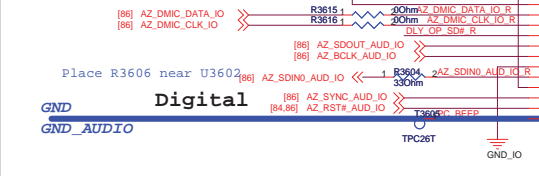
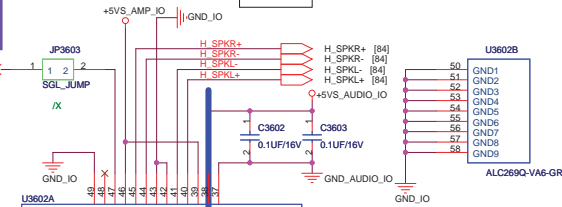
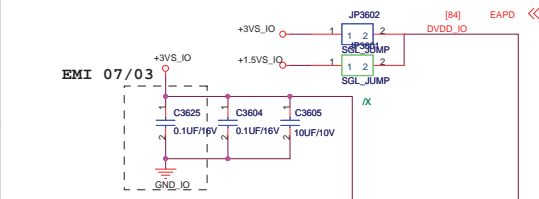
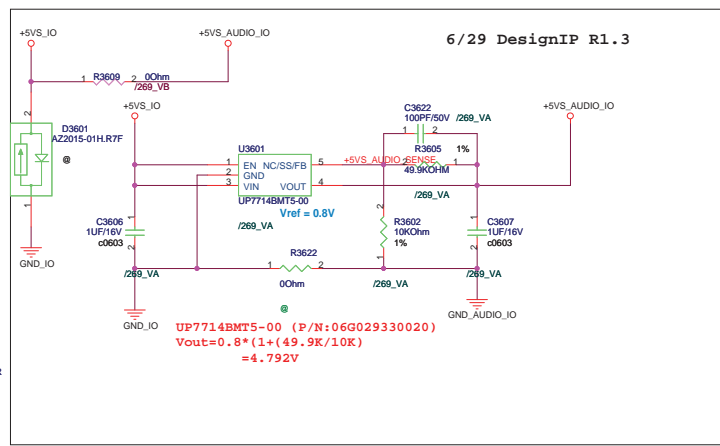
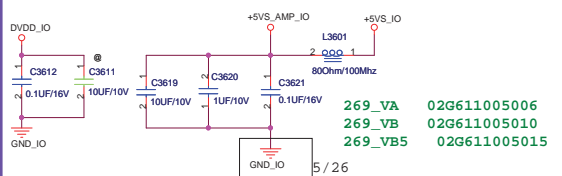
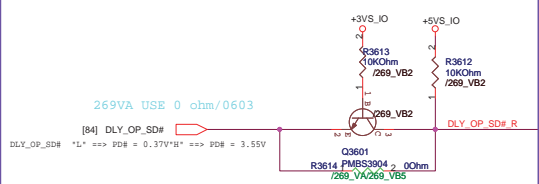
For POWER ON LED



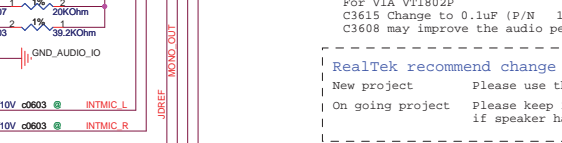
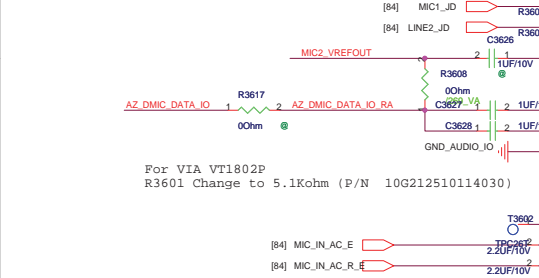
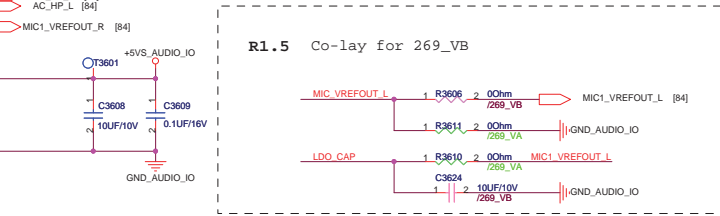
0521:change +5V_USB_IO to +5VSUS_IO

		Title :PWR_BUTTON_LED	
ASUSTEK COMPUTER INC		Engineer: <i>Anndy_wang</i>	
Size A	Project Name 1215N_IO		Rev 1.3
Date	Sheet 82 of 92		

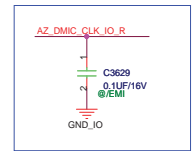
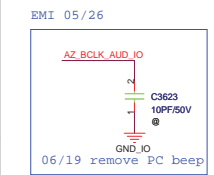
R1.7 ALC269-VB2 Issue
 PD# is internal pull-up to 5VS_AUDIO & VIH=3.3V
 Add R3602 & R3613 of PD# to make sure the PD# is higher than 3.3V when power up speaker amplifier



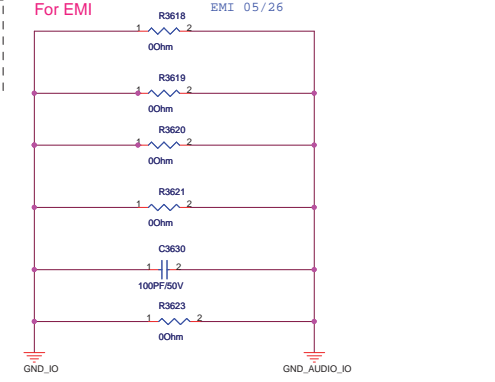
For VIA VT1802P
 C3627 C3628 Change to 2.2UF/10V (P/N 11G233322536360)

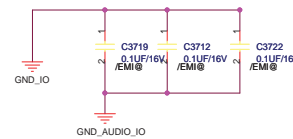
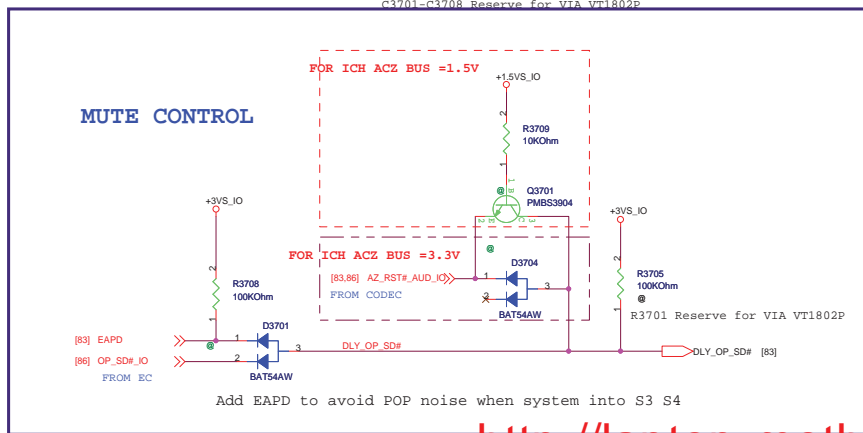
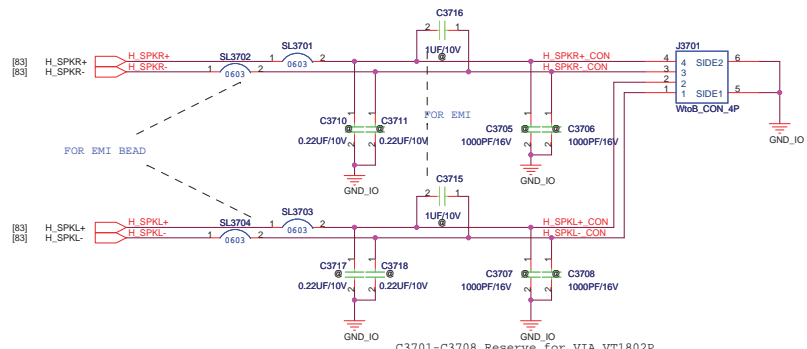
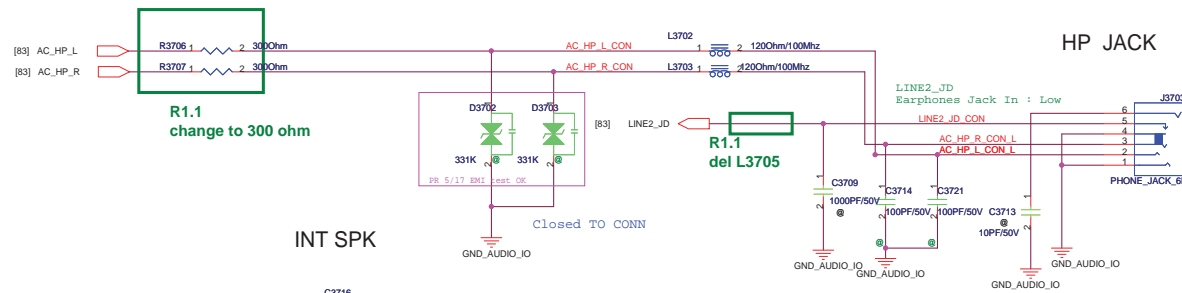
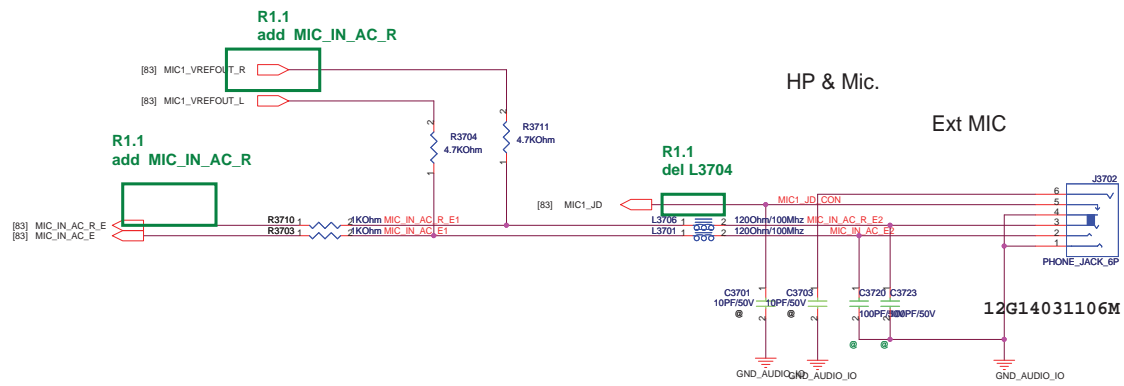


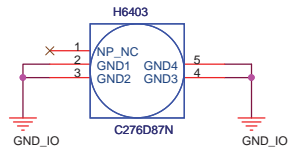
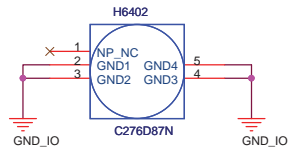
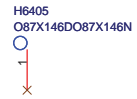
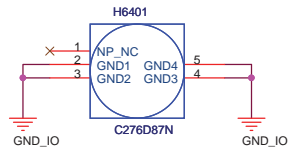
RealTek recommend change C3615 from 2.2uF to 1uF
 New project Please use the 1uF for VREF_CODECD
 On going project Please keep 2.2uF for VREF_CODECD
 if speaker have not S3 S4 resume issue.

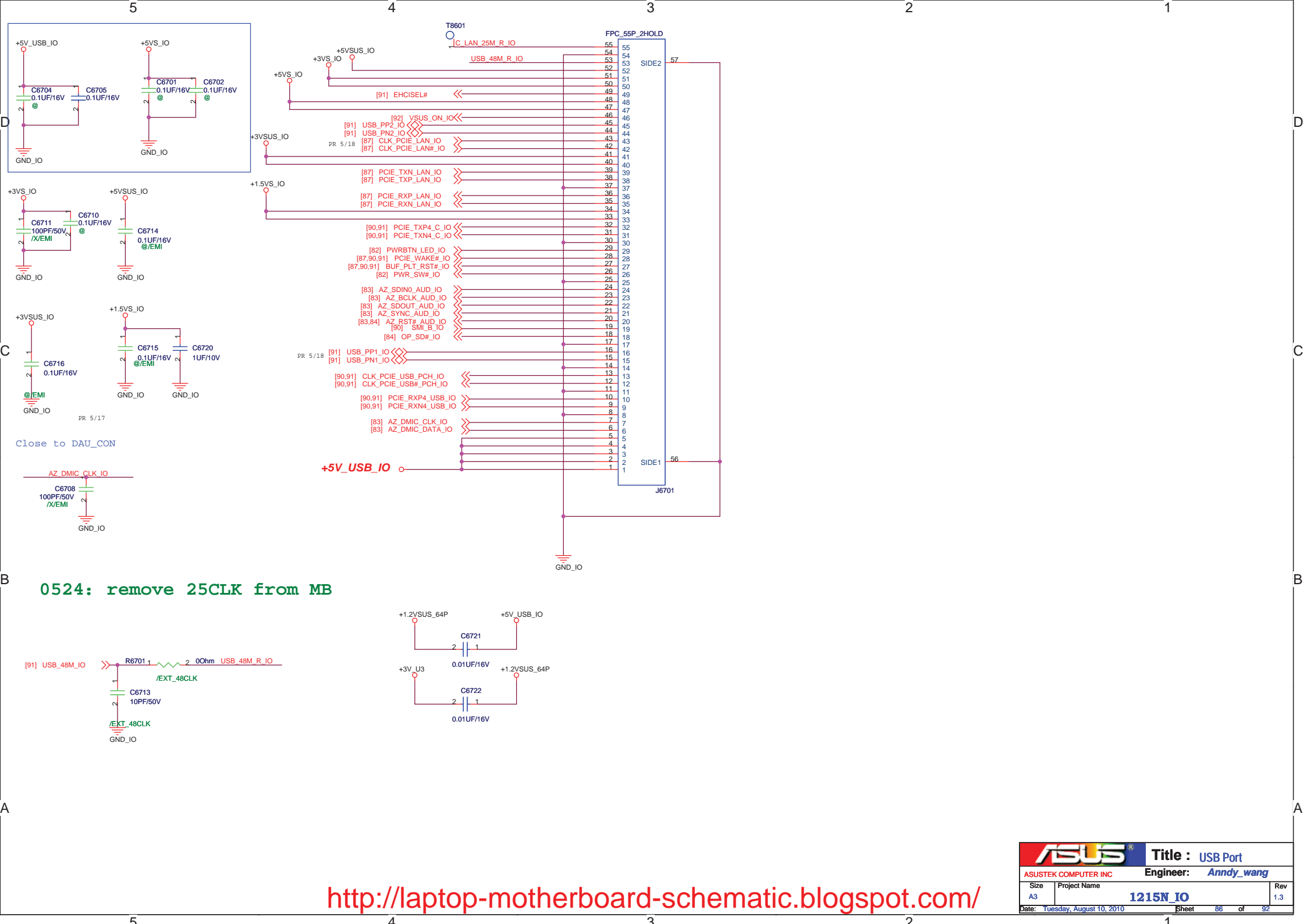


For VIA VT1802P
 Please reserve 11G232022004320 for ACZ_BCLK_AUD at PCH (SB) side





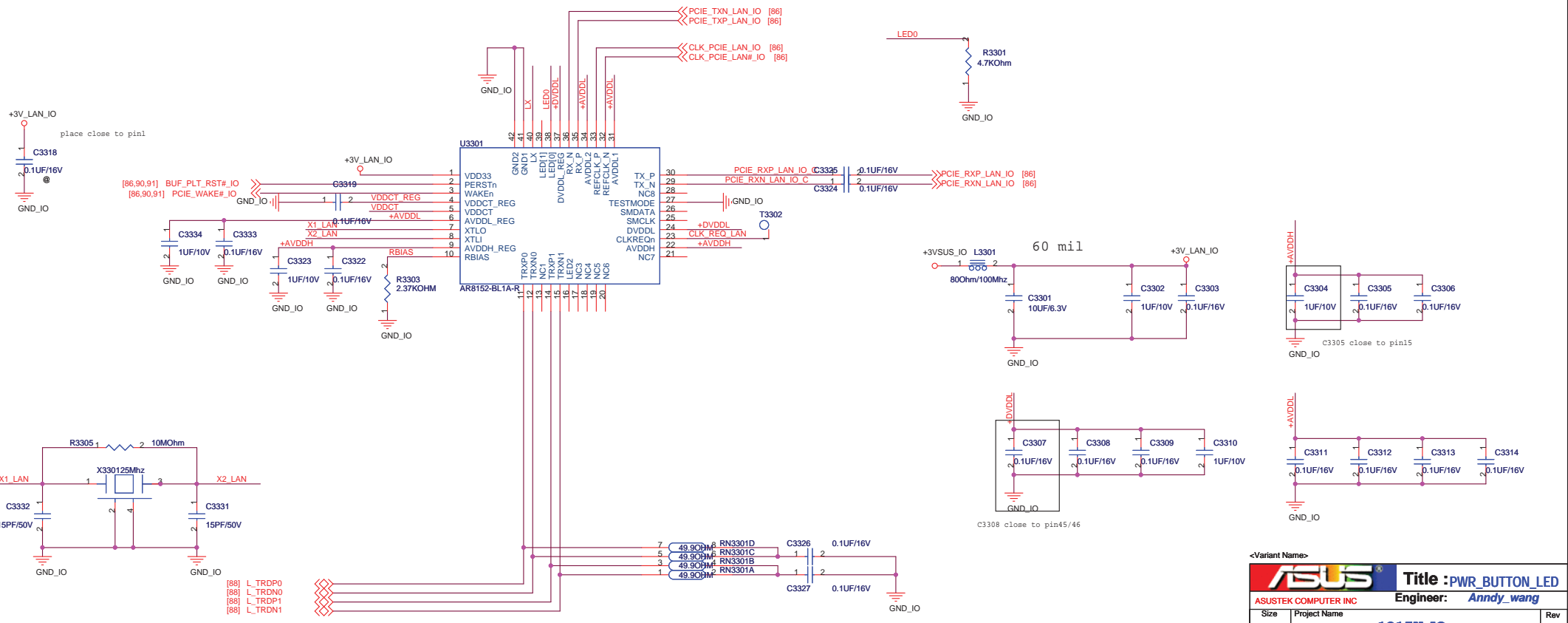
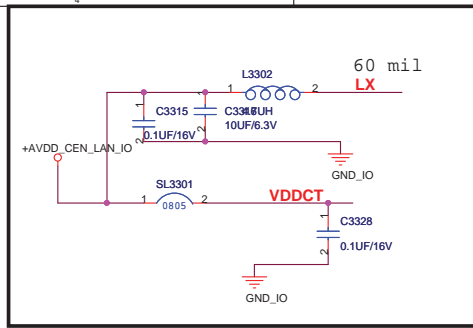




0524: remove 25CLK from MB

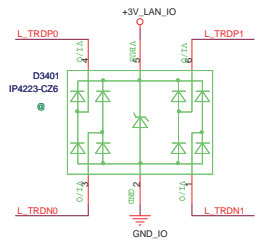
<http://laptop-motherboard-schematic.blogspot.com/>

		Title : USB Port	
ASUSTEK COMPUTER INC		Engineer: Anndy_wang	
Size	Project Name	Rev	
A3	1215N_IO	1.3	
Date: Tuesday, August 10, 2010		Sheet 86 of 92	

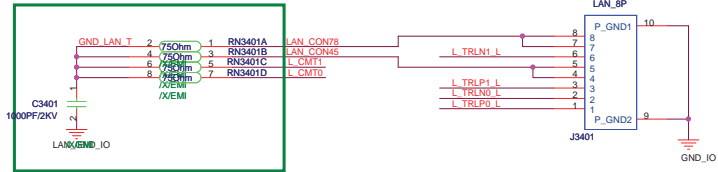
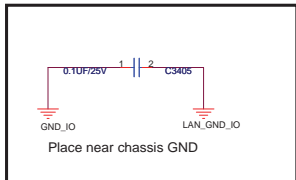
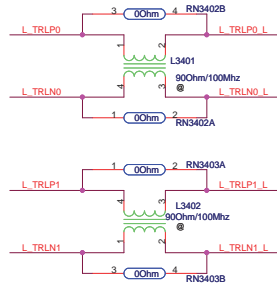
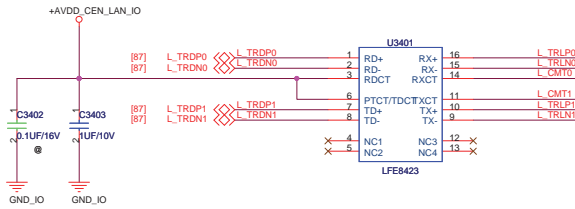


<Variant Name>

ASUS		Title : PWR_BUTTON_LED	
ASUSTEK COMPUTER INC		Engineer: Anndy_wang	
Size	Project Name	Rev	
Custom	1215N_IO	1.3	
Date: Tuesday, August 10, 2010		Sheet	87 of 92



GND_LAN_T 窺わ ヅ : 策ン



R.1.1 EMI

5

4

3

2

1

D

D

C

C

B

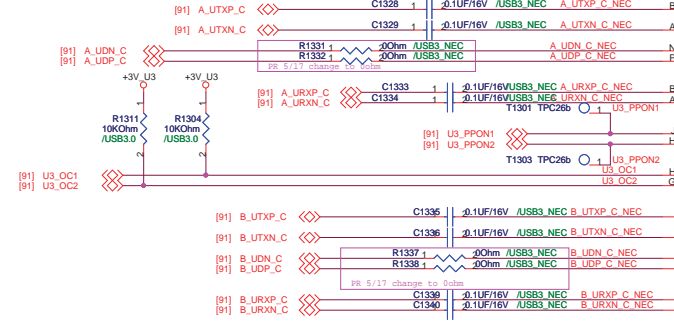
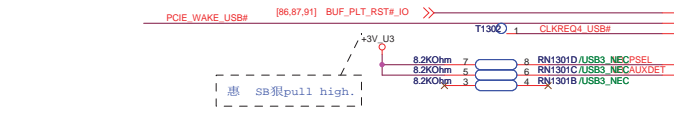
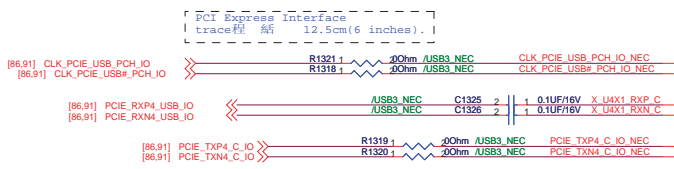
B

A

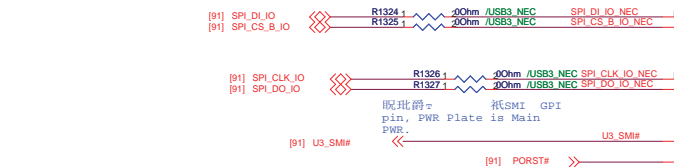
A

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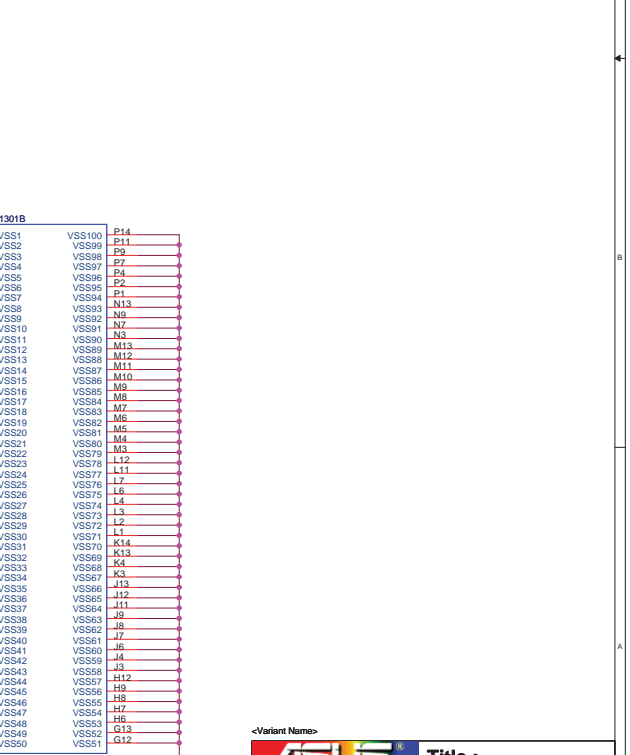
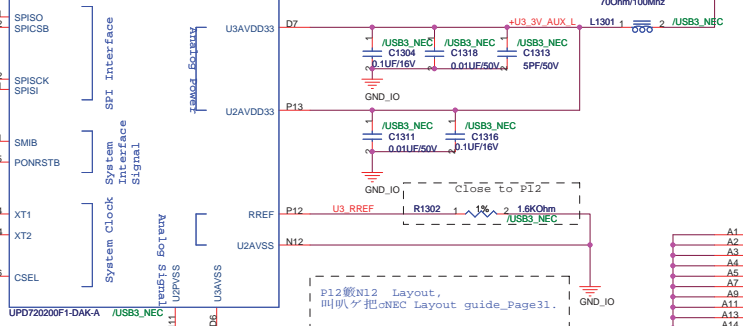
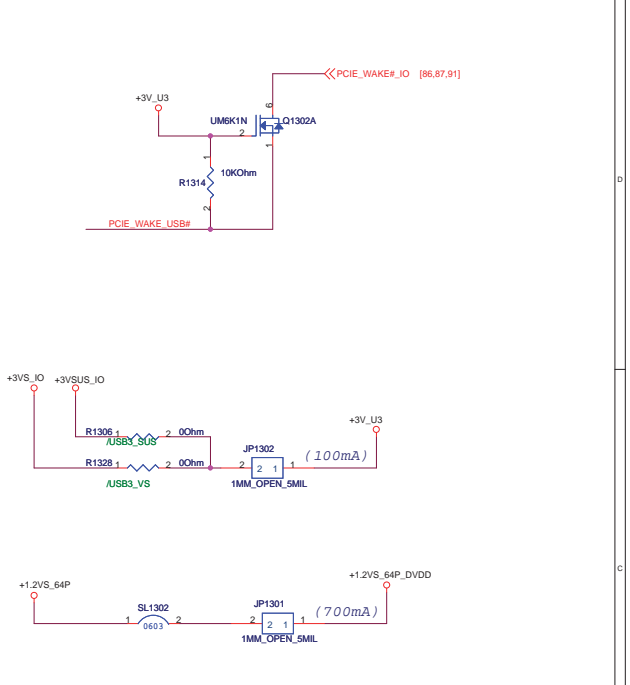
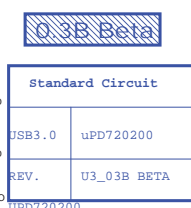
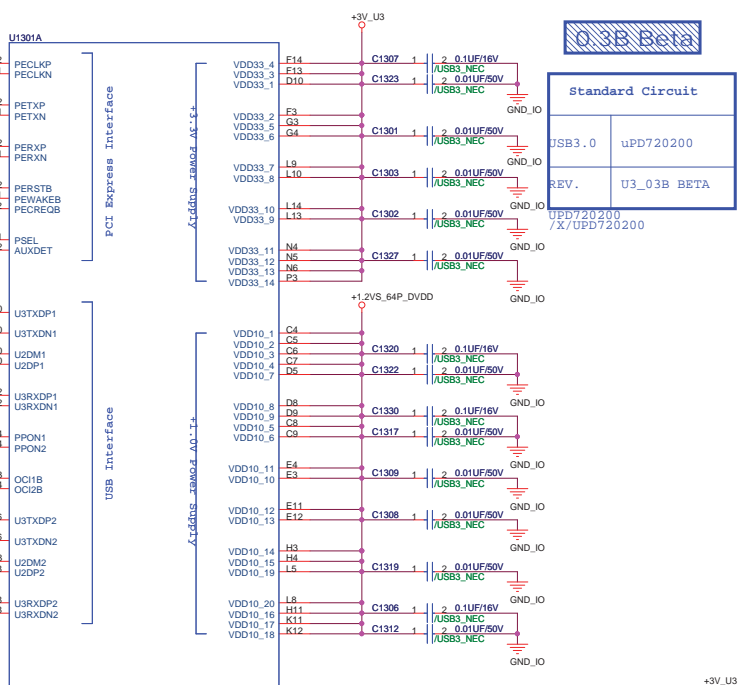
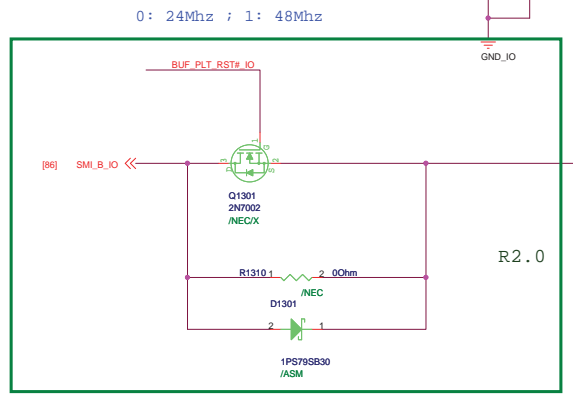
		Title : EMI	
ASUSTEK COMPUTER INC		Engineer: Anndy_wang	
Size	Project Name	Rev	
A3	1215N_IO	1.3	
Date: Tuesday, August 10, 2010	Sheet	89	of 92

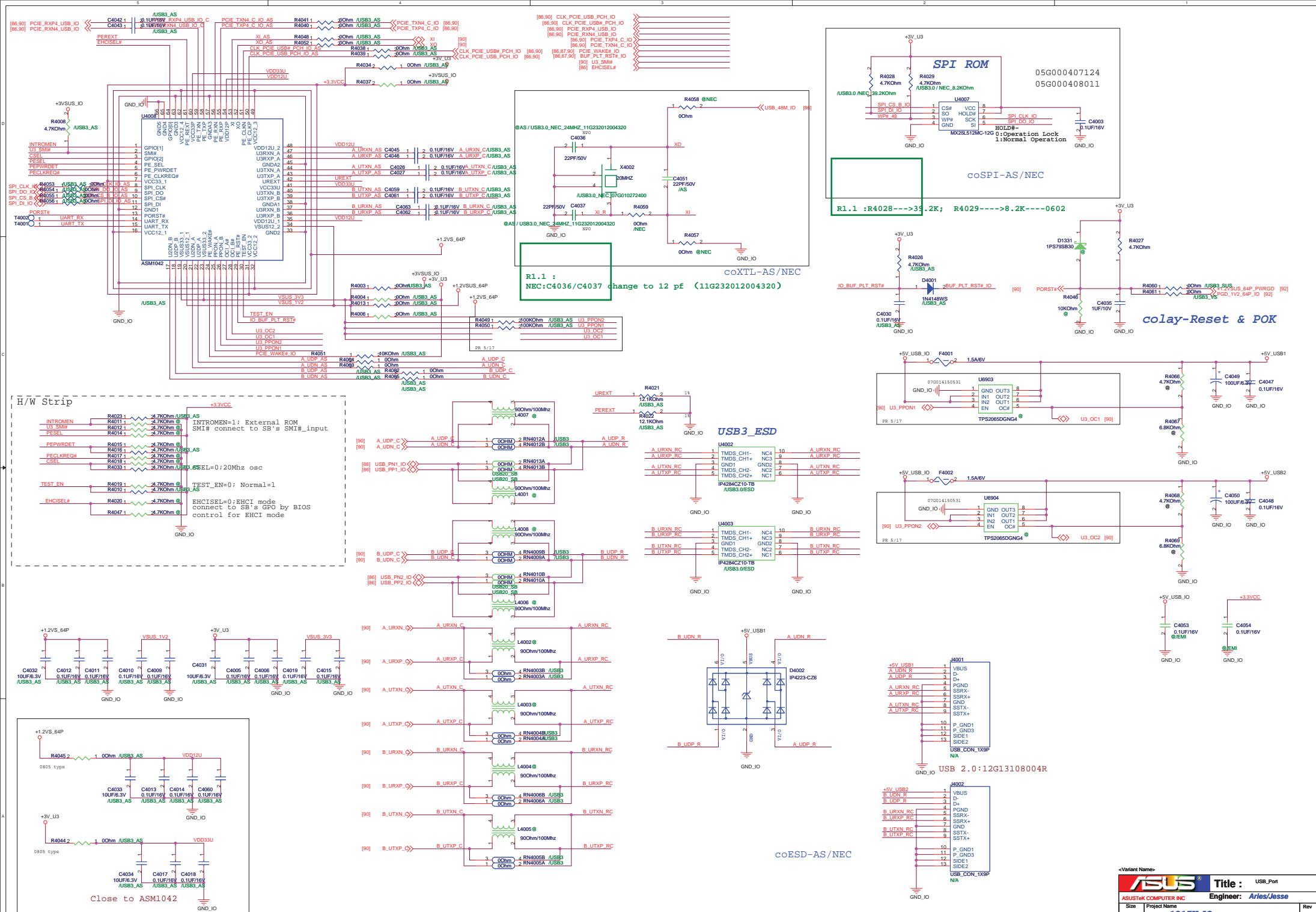


(1) USB3.0 Interface trace程 統 10cm(4 inches).
(2) USB Interface differential trace tolerance = 0.12mm(5 mail).

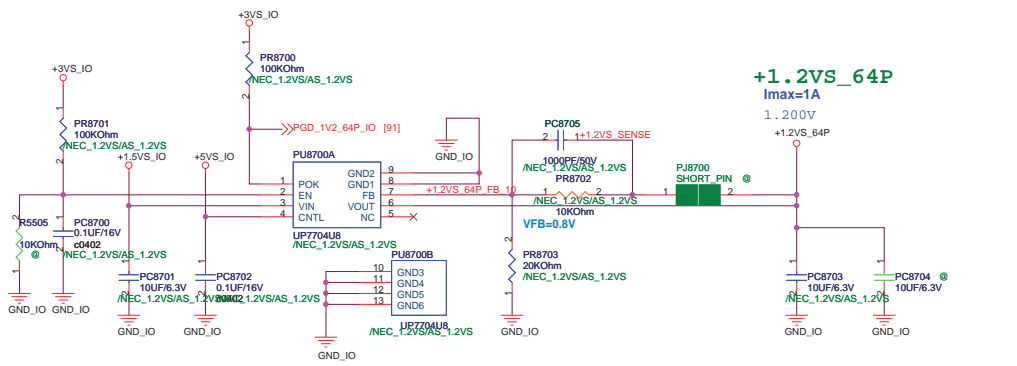


铜 场 块 48Mhz Clock.
瑞 瑞 一 个 Clock,
叫 把 USB3.0 datasheet.

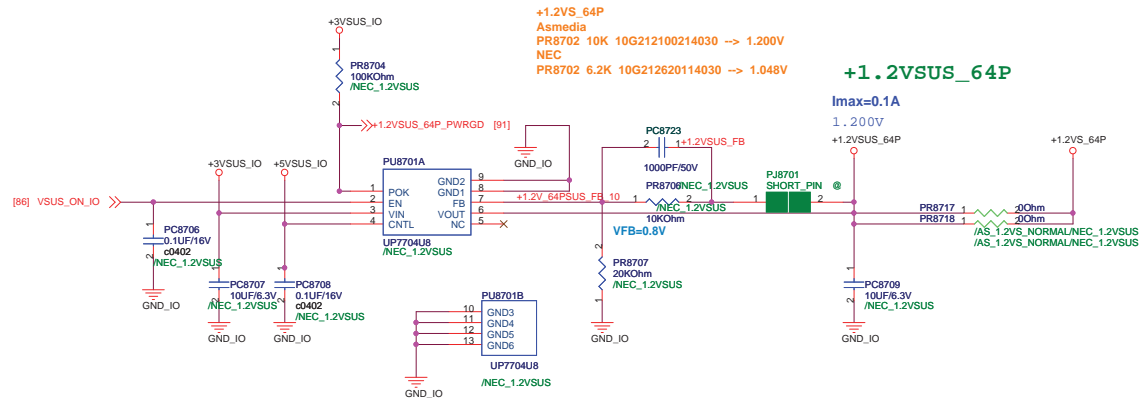




<http://laptop-motherboard-schematic.blogspot.com/>



Dual_layout BOM_table	OPTIONAL CHOICE	Voltage(NEC=1.05V;ASM=1.2V)
NEC (Normal)	/NEC_1.2VS/AS_1.2VS	NEC PR8702 6.2K 10G212620114030 --> 1.048V
NEC(SUS)	/NEC_1.2VSUS	NEC PR8706 6.2K 10G212620114030 --> 1.048V
ASM1042(Normal)	/NEC_1.2VS/AS_1.2VS /AS_1.2VS_ALL NORMAL	Asmedia PR8702 10K 10G212100214030 --> 1.200V
ASM1042(Normal +SUS)	/NEC_1.2VS/AS_1.2VS /NEC_1.2VSUS	Asmedia PR8702 10K 10G212100214030 --> 1.200V Asmedia PR8706 10K 10G212100214030 --> 1.200V



Dual_layout BOM_table	BOM(USB interface)	BOM(PCIe interface)	BOM(XTL interface)	BOM(SPI interface)
ASM only (USB3.0) (USB2.0)	C4045, C4046, C4026, C4027, C4059, C4061, C4062, C4063, C4064, C4065, C4066, C4067, RN4012A, RN4012B	R4038, R4039, R4040, R4041, C4042, C4043	X4002(20MHZ, 07G010012000), @C4036, C4037(22pF,11G232022004030), C4051, R4032, @C4052	R4053, R4054, R4055, R4056, R4028/ R4029 (4.7K, 10G212472004030), C4003, U4007
NEC only (USB3.0) (USB2.0)	C1328, C1329, C1331, C1332, C1333, C1334, C1335, C1336, C1337, C1338, C1339, C1340, RN4012A, RN4012B	R1318, R1319, R1320, R1321, C1325, C1326	X4002(24MHZ,11G232027004070), C4036,C4037(12pF,11G232012004320), @C4051, R1317, @R1315, @R1316	R1324, R1325, R1326, R1327, R4028(8.2K, 10G212822004030), R4029(39.2K, 10G212392214031), C4003, U4007
PCH only (USB2.0)	RN4013A, RN4013B			
ASM+PCH (USB3.0) (USB2.0)	C4045, C4046, C4026, C4027, C4059, C4061, C4062, C4063, C4064, C4065, C4066, C4067, RN4012A, RN4012B, RN4013A, RN4013B	R4038, R4039, R4040, R4041, C4042, C4043		
NEC+PCH (USB3.0) (USB2.0)	C1328, C1329, C1331, C1332, C1333, C1334, C1335, C1336, C1337, C1338, C1339, C1340, RN4012A, RN4012B, RN4013A, RN4013B	R1318, R1319, R1320, R1321, C1325, C1326		

<Variant Name>


ASUS		Title : N/A	
ASUSTeK COMPUTER INC. NB		Engineer: Aaron_Lin	
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1.3G

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- 01. Block Diagram
- 02. PWR_BUTTON_LED
- 03. ALC269-1
- 04. ALC269-2(I/O)
- 05. ALC269-3(I/O)
- 06. DAU_HDD_CON
- 07. LAN
- 08. LAN CONN.
- 09. USB3.0_ASM1042
- 10. USB_Port
- 11. Srew Hole
- 12. EMI

		Title : Block Diagram	
ASUSTek Computer INC.		Engineer: ERICH_LEE	
Size	Project Name	Rev	
A4	1215N_IO	1.3	
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